CCS Technical Documentation
RH-48 Series Transceivers

Troubleshooting – BB

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Contents

Baseband Troubleshooting

RH-48 Baseband Module Overview

The Baseband module of the RH-48 transceiver is a CDMA single-band engine. The baseband architecture is based on the DCT4 Apollo engine.

RH-48 cellular baseband consists of three ASICs: Universal Energy Management (UEM), Universal Phone Processor (UPP), and a 128/8 megabit combo FLASH.

The baseband architecture supports a power-saving function called *sleep mode*. This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode, the system runs from a 32 kHz crystal and all the RF regulators (VR1A, VR1B, VR2, ... VR7) are off. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock is switched off. The phone is waken up by a timer running from this 32 kHz clock supply. The period of the sleep/wake up cycle (slotted cycle) is 1.28N seconds, where N= 0, 1, 2, depending on the slot cycle index.

RH-48 supports standard Nokia 2-wire and 3-wire chargers (ACP-x and LCH-x). However, the 3-wire chargers are treated as 2-wire chargers. The PWM control signal for controlling the three-wire charger is ignored. UEM ASIC and EM SW control charging.

BL-5C Li-ion battery is used as main power source for RH-48. BL-5C has nominal capacity of 850 mAh.

Baseband and RF Architecture

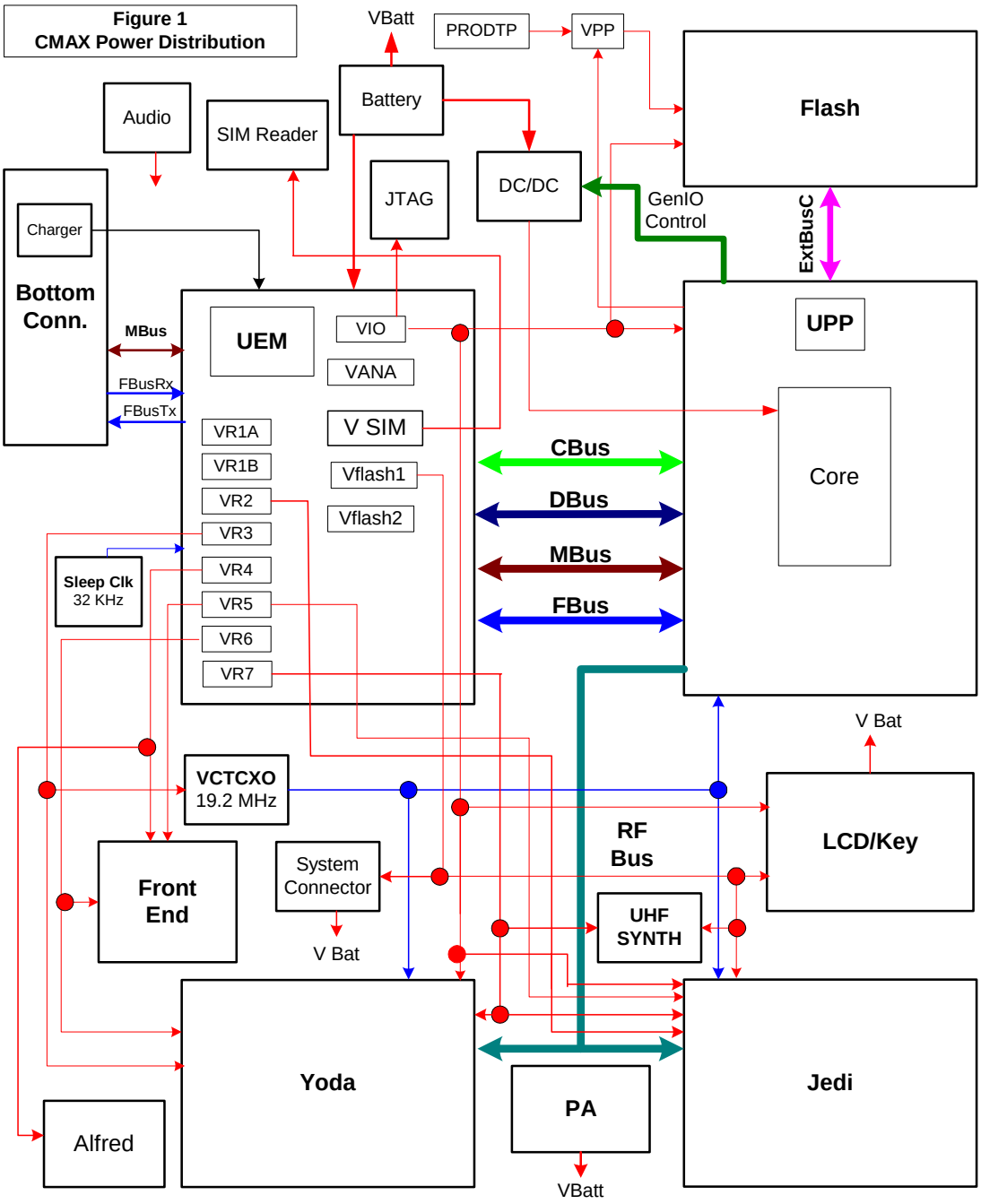


Figure 1: RH-48 Power Distribution Diagram

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. RH-48 baseband can be powered up in the following ways:

- By the Power button, which means grounding the PWRONX pin of the UEM
- By connect the charger to the charger input
- By the RTC Alarm, when the RTC logic has been programmed to give an alarm.

After receiving one of the above signals, the UEM counts a 20ms delay and then enters its reset mode. The watchdog starts up, and if the battery voltage is greater than Vcoff+, a 200ms delay is started to allow references, etc. to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500us later VR3, VANA, VIO, and VCORE are enabled. Finally the Power Up Reset (PURX) line is held low for 20 ms. This reset, PURX, is sent to UPP; resets are generated for the MCU and the DSP. During this reset phase, the UEM forces the VCTCXO regulator on — regardless of the status of the sleep control input signal to the UEM. The FLSRSTx from the UPP is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on at the UEM power on — except for the SIM regulator and Vflash2. Vsim and Vflash2 are not used. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

The following timing diagram represents UEM start-up sequence from reset to power-on mode.

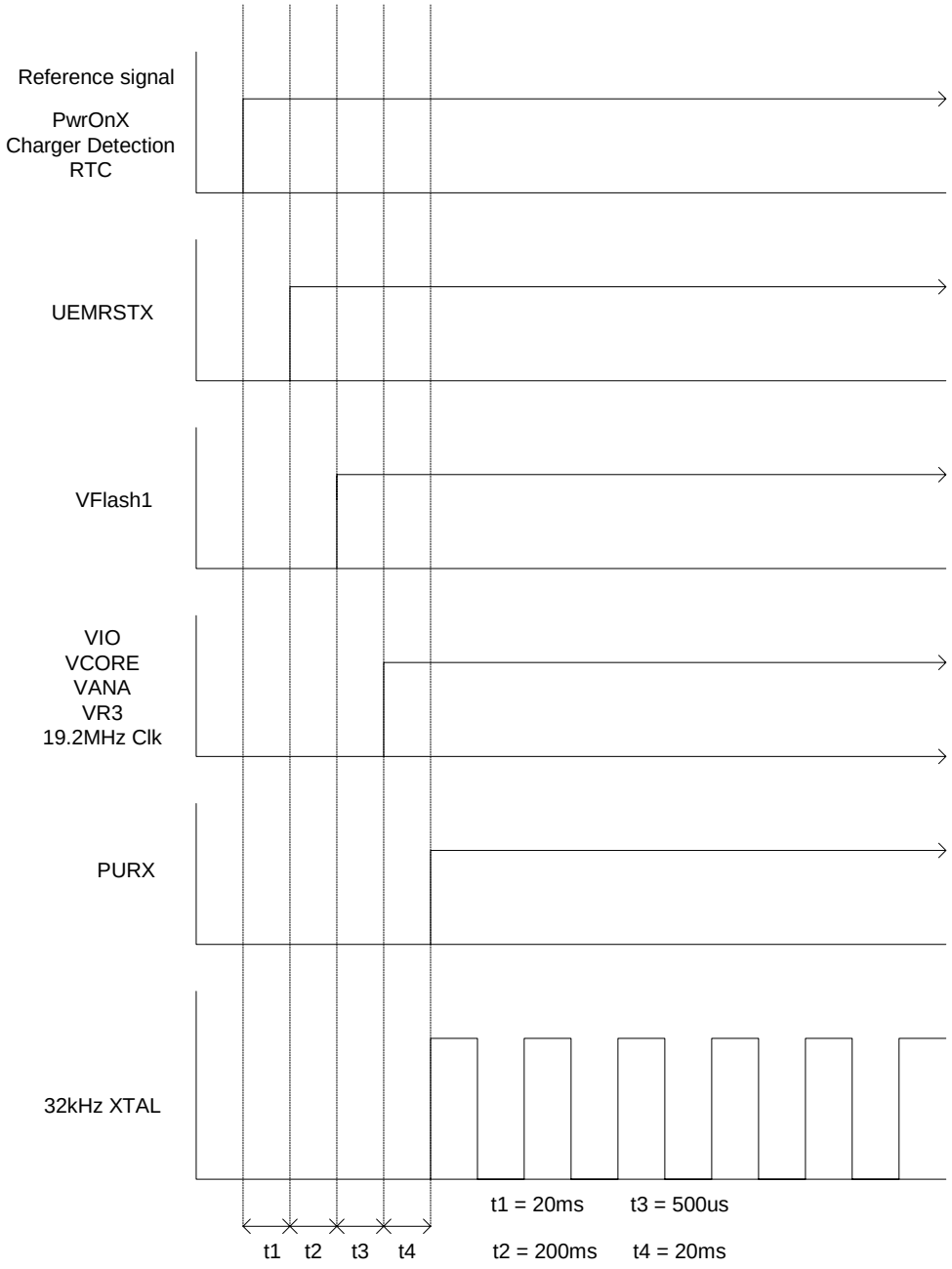


Figure 2: Power on sequence and timing

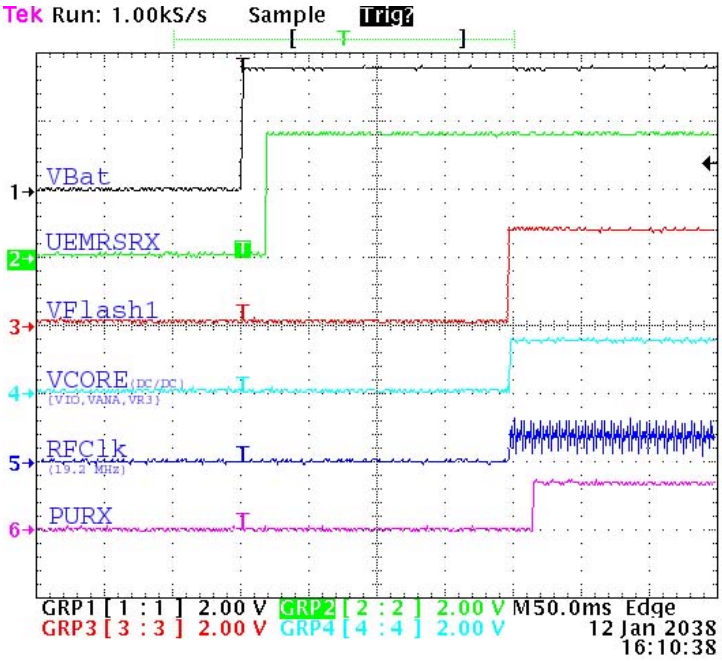


Figure 3: Measured power on sequence and timing

Power up with PWR key

When the Power on key is pressed, the UEM enters the power-up sequence. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notice that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power-on situation, the MCU powers off the baseband.

Power up when charger is connected

In order to be able to detect and start charging in cases where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by *START-UP CHARGING* circuitry.

Whenever VBAT level is detected to be below master reset threshold (V_{MSTR-}), charging is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above charger detection threshold, VCH_{DET+}. By detection start-up charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As battery charges its voltage rises, and when VBAT voltage level higher than master reset threshold limit (V_{MSTR+}) is detected START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). MSTRX='1' output reset signal (internal to UEM) is given to UEM's *RESET* block when VBAT>V_{MSTR+} and UEM enters into reset sequence.

If VBAT is detected to fall below V_{MSTR} during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCH_{DET+}).

RTC alarm power up

If phone is in POWER_OFF mode when RTC alarm occurs the wake-up procedure. After baseband is powered on, an interrupt is given to MCU. When RTC alarm occurs during ACTIVE mode, the interrupt for MCU is generated.

Power off

The Baseband switch power-off mode if any of following statements is true:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Watchdog timer register expires

The Power-down procedure is controlled by the UEM.

Power Consumption and Operation modes

In the POWER-OFF mode, the power (VBAT) is supplied to UEM, buzzer, vibra , LED, PA and PA drivers (Tomcat and Hornet). During this mode, the current consumption on this mode is approximately 35uA.

In the SLEEP mode, both processors, MCU and DSP, are in stand-by mode. Phone will go to sleep mode only when both processors make this request. When SLEEPX signal is detected low by the UEM, the phone enters SLEEP mode. VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode, and VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When SLEEPX signal is detected high by the UEM, the phone enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection, etc.

In sleep mode, VCTCXO is shut down and 32 kHz sleep clock oscillator is used as reference clock for the baseband.

The average current consumption of the phone in sleep mode can vary depending mainly on SW state (e.g., slot cycle 0, 1, or 2 and if the phone is working on IS95 or IS2000 for CDMA); however, on average is about 6 mA in slot cycle 0 on IS95.

In the ACTIVE mode, the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the phone present state of the phone such as: burst reception, burst transmission, if DSP is working, etc.

In active mode SW controls the UEM RF regulators: VR1A and VR1B can be enabled or disabled. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8V or 3.3V. VR2 and VR4 -VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during Sleep mode and cannot be control by SW in the same way as the other regulators. VR3 will only turn off if both processors request to be in sleep mode.

In the CHARGING mode, the charging can be performed in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size, and charging current are measured by the UEM, and the charging software running in the UPP controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery and phone. The battery voltage rise is limited by turning the UEM switch off, when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell capacity of 850 mAh, and some safety and protection circuits to prevent harm to the battery.

The UEM ASIC controls the power distribution to the whole phone through the BB and RF regulators excluding the power amplifier (PA), which has a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system: UEM, PA, buzzer, vibra, display, and keyboard lights.

The heart of the power distribution to the phone is the power control block inside UEM. It includes all the voltage regulators and feeds the power to the whole system. UEM handles hardware functions of power up so that regulators are not powered and power up reset (PURX) are not released if battery voltage is less than 3 V.

RH-48 Baseband is powered from five different UEM regulators (VANA, VIO, VFLASH1, VFLASH2, and VCORE (DC/DC) See Table 1.

UEM supplies also voltages VR1A, VR1B, VR2, VR3, VR4, VR5, VR6, and VR7 for RF. See Table 2.

Table 1: RH-48 Baseband regulators

Regulator	Maximum current (mA)	Vout (V)	Notes
VCORE	300	1.5	Output voltage selectable 1.0V/1.3V/1.5V/1.8V Power up default 1.5V
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (Off during sleep and power off-modes)
VSIM	25	3.0	Enabled only when SIM card is used

Table 2: RH-48 RF regulators

Regulator	Maximum current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell transmitter is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

The charge pump that is used by VR1A is constructed around UEM. The charge pump works with Cbus (1.2 MHz) oscillator and gives a 4.75 V regulated output voltage to RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator VCTCXO (G500). This 19.2 MHz clock signal is generated at the RF and is fed to Yoda pin 18 (TCXO_IN). Yoda then converts the analog sine wave-form to a digital waveform with swing voltage of 0 tot 1.8V and sends it to the UPP from pin 16 at Yoda (19.2 Out) to the UPP pin M5 (RFCLK). (See Figure 4 for waveform.)

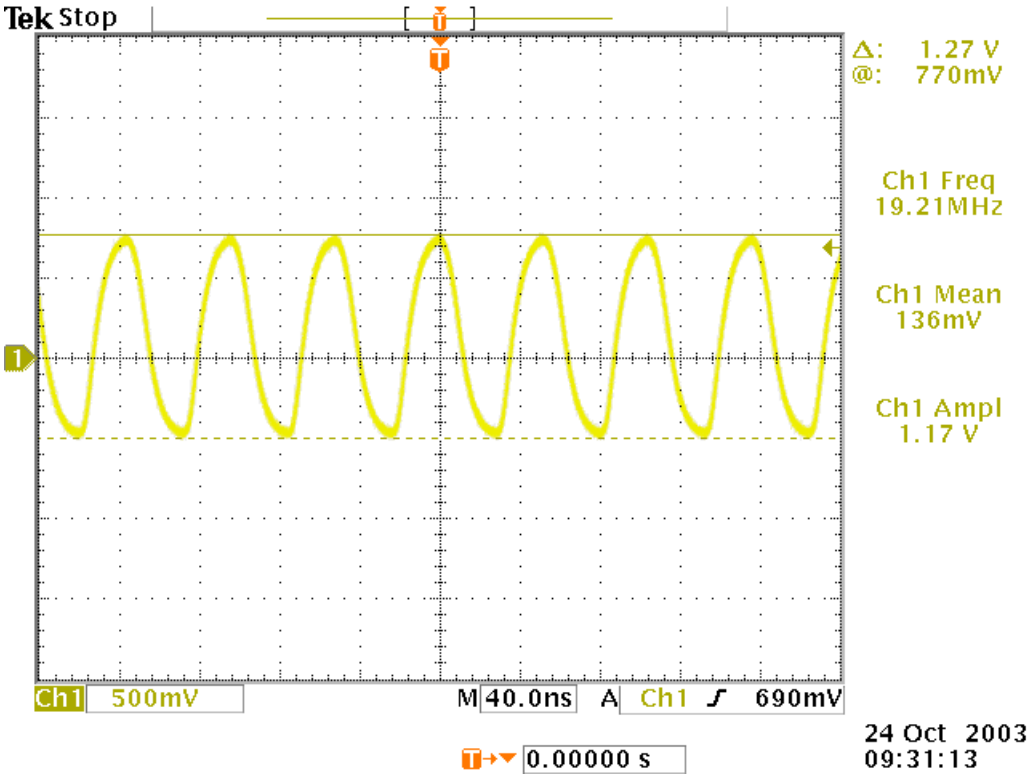


Figure 4: Waveform of 19.2MHz clock (VCTCXO) going to the Yoda ASIC

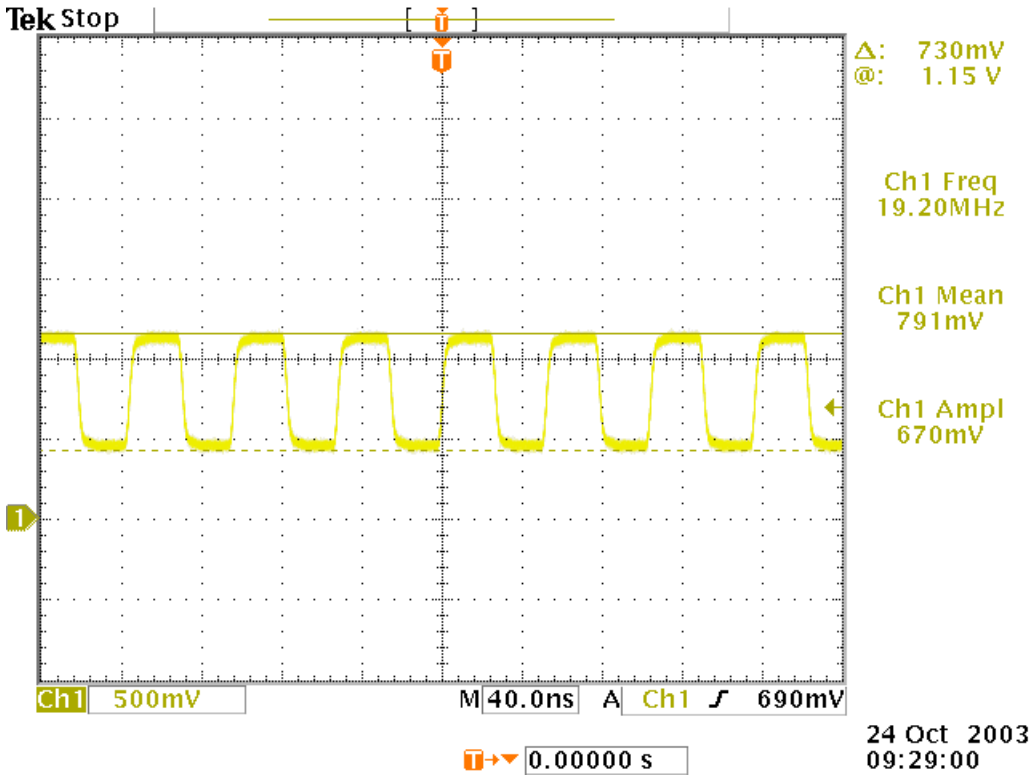


Figure 5: Waveform of 19.2MHz Clk going to the UPP for Yoda ASIC at C711

This is the RFCLK signal for the UPP.

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2MHz internal clock to the DSP and MCU, where SW multiplies this clock by seven for the DSP and by two for the MCU. (See Figure 6.)

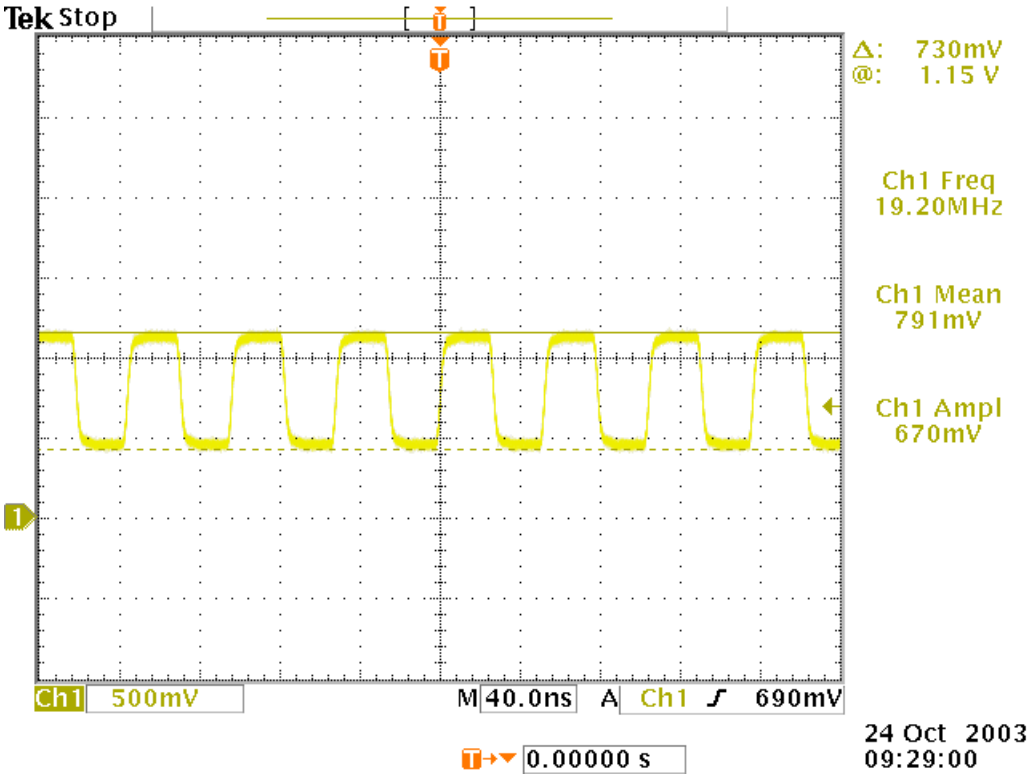


Figure 6: RFCovCLk waveform

CBUSClk Interface

A 1.2 MHz clock signal is use for CBUS, which is used by the MCU to transfer data between UEM and UPP. (See the following figure for Cbus data transfer.)

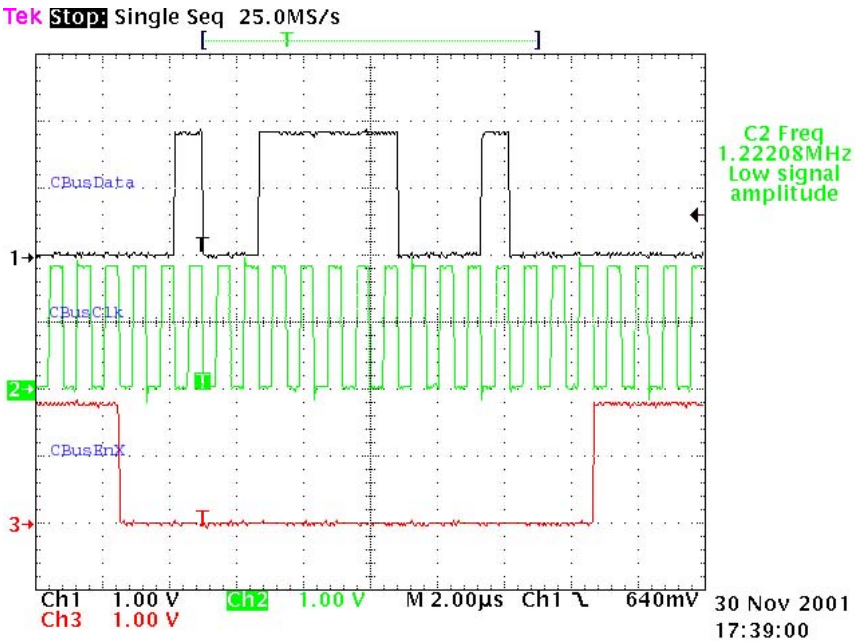


Figure 7: Cbus Data Transfer

DBUS Clk Interface

A 9.6 MHz clock signal is use for DBUS, which is used by the DSP to transfer data between UEM and UPP. (See the following figure.)

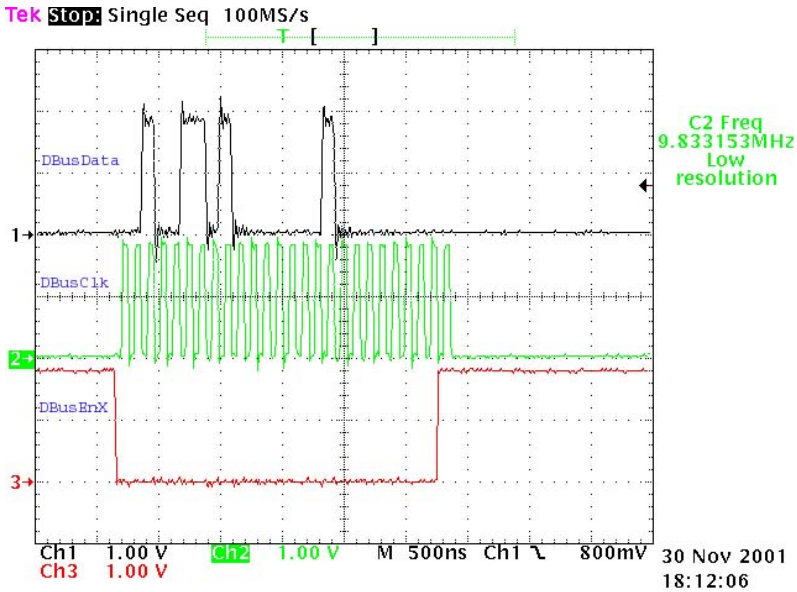


Figure 8: Dbus data transferring

The system clock is stopped during sleep mode by disabling the VCTCXO power supply (VR3) from the UEM regulator output by turning off the controlled output signal SleepX from UPP.

SleepCLK (Digital)

The UEM provides a 32kHz sleep clock for internal use and to UPP, where it is used for the sleep mode timing. (Figure 9.)

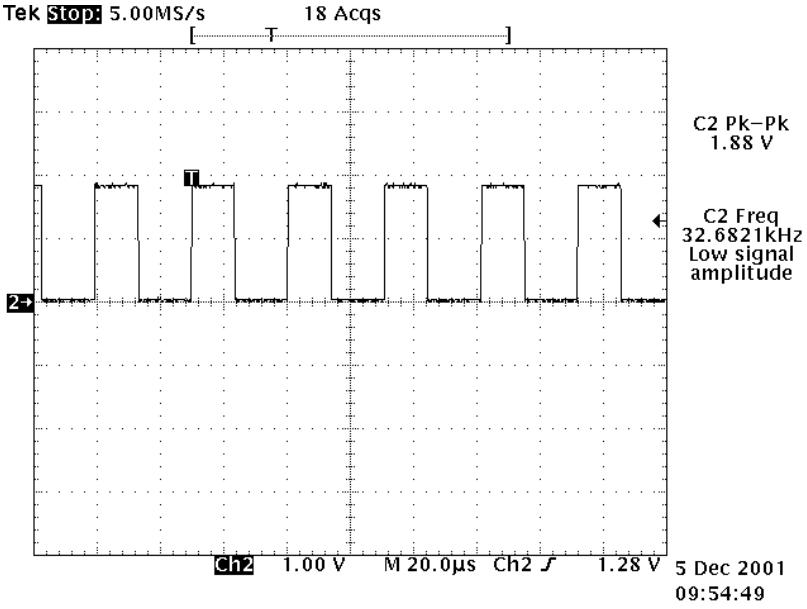


Figure 9: 32kHz Digital output from UEM

SleepCLK (Analog)

However, when the system enters sleep mode or power off mode, the external 32KHz crystal provides a reference to the UEM RTC circuit to turn on the phone during power off or sleep mode. (Figure 10.)

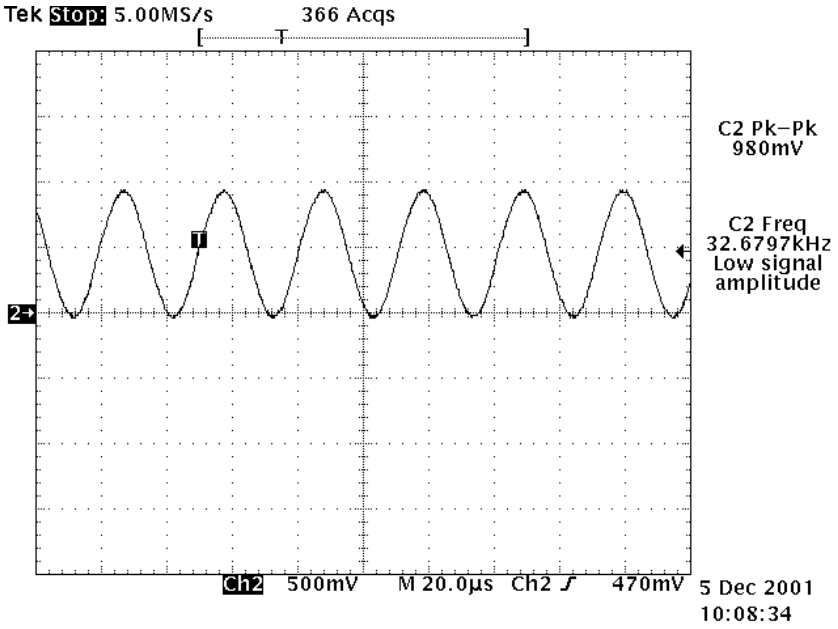


Figure 10: 32kHz analog waveform at 32KHz crystal input

Flash programming

Connections to Baseband

The Flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface uses the VPP, FBUSTX, FBUSRX, MBUS, and BSI connections for the connection to the baseband. The connection is through the UEM, which means that the logic levels are corresponding to 2.7V. Power is supplied using the battery contacts.

Baseband Power Up

The baseband power is controlled by the flash prommer in production and in re-programming situations. Applying supply voltage to the battery terminals the baseband will power up. Once the baseband is powered, flash-programming indication is done as described in the following section.

Flash Programming Indication

Flash programming is indicated to the UPP using MBUSRX signal between UPP and UEM. The MBUS signal from the baseband to the flash prommer is used as clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot to indicate that the flash prommer is connected. If the UPP MBUSRX signal is low on UPP, the MCU enters flash programming mode. In order to avoid accidental entry to the flash-programming mode, the MCU only waits for a specified time to get input data from

the flash prommer. If the timer expires without any data being received, the MCU will continue the boot sequence. The MBUS signal from UEM to the external connection is used as clock during flash programming. This means that flash-programming clock is supplied to UPP on the MBUSRX signal.

The flash prommer indicates the UEM that flash programming/reprogramming by writing an 8-bit password to the UEM. The data is transmitted on the FBUSRX line and the UEM clocks the data on the FBUSRX line into a shift register. When the 8 bits have been shifted in the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content in the UEM into a compare register. If the 8 bits in the compare registers matches with the default value preset in the UEM, the flash prommer shall pull the MBUS signal to UEM low in order to indicate to the MCU that the flash prommer is connected. The UEM reset state machine performs a reset to the system, PURX low for 20 ms. The UEM flash programming mode is valid until MCU sets a bit in the UEM register that indicates the end of flash programming. Setting this bit also clears the compare register in the UEM previously loaded at the falling edge of the BSI signal. During the flash programming mode the UEM watchdogs are disabled. Setting the bit indicating end of flash programming enables and resets the UEM watchdog timer to its default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP.

The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register, the BSI signal will be gated during UEM master reset and during power on when PURX is active. The BSI signal should not change state during normal operation unless the battery is extracted; in this case, the BSI signal will be pulled high, note a falling edge is required to load the compare register.

Flashing

- Flash programming is done through VPP, FBUSTX, FBUSRX, MBUS, and BSI signals.
- When phone has entered the flash programming mode, the prommer indicates to UEM that flash programming will take place by writing 8-bit password to UEM. The prommer sets BSI to “1” and then uses FBUSRX for writing and MBUS for clocking. After that, BSI is set back to “0”.
- MCU indicates to prommer that it has been noticed, by using the FBUSTX signal. After this, it reports UPP type ID and is ready to receive secondary boot code to its internal SRAM.

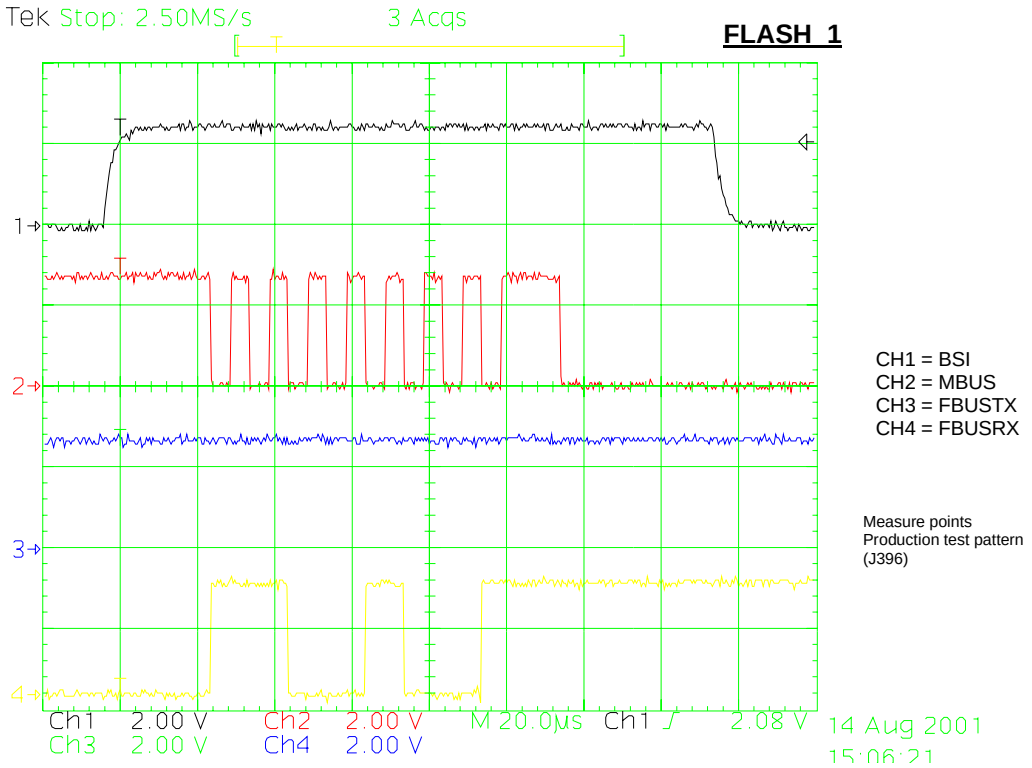


Figure 11: Flashing starts by BSI being pulled up and password being sent to UEM

- This boot code asks MCU to report prommer phone's configuration information, including flash device type. Now prommer can select and send algorithm code to MCU SRAM (and SRAM/Flash self-tests can be executed).

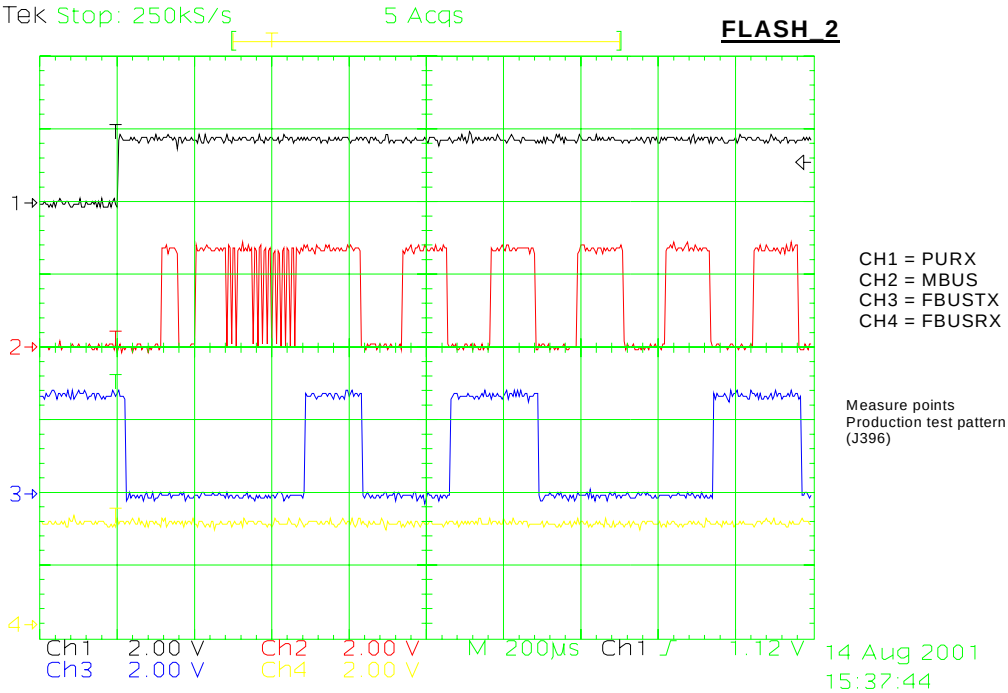


Figure 12: Flashing, continued

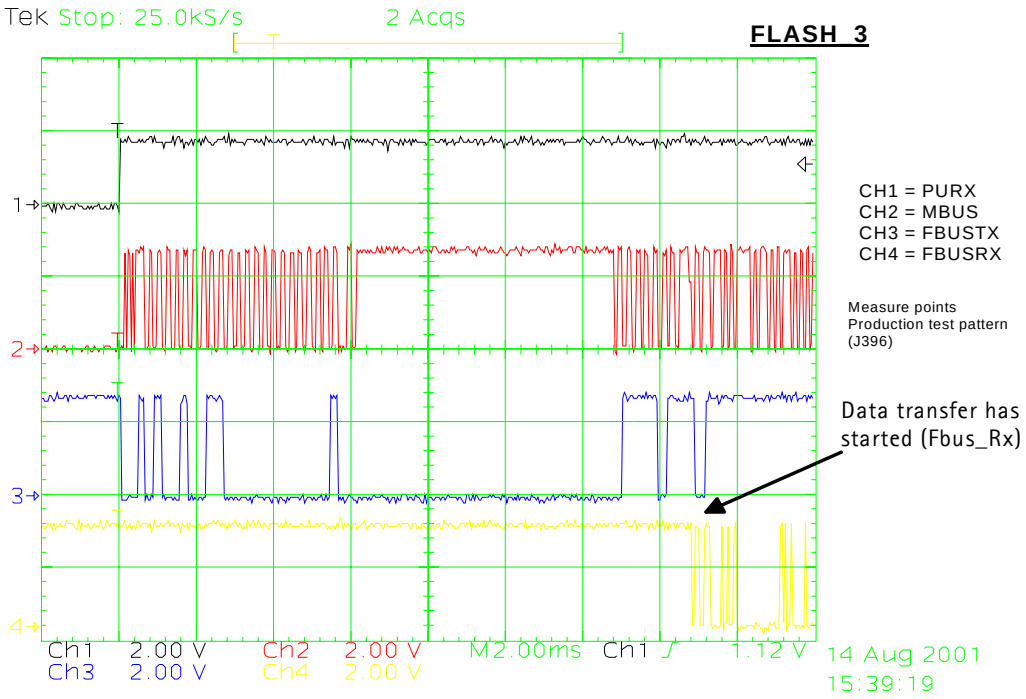


Figure 13: Flashing, continued

Charging operation

Battery

In RH-48, a Lithium-Ion cell battery with a capacity of 850 mAh is used. Reading a resistor inside the battery pack on the BSI line indicates the battery size. With an NTC resistor on PWB, the phone measures the approximate temperature of the battery on the BTEMP line.

Temperature and capacity information are needed for charge control. These resistors are connected to BSI pin of the battery connector and BTEMP of the phone. Phone has 100 kΩ pull-up resistors for this line so that they can be read by A/D inputs in the phone.

See the following figures for details.

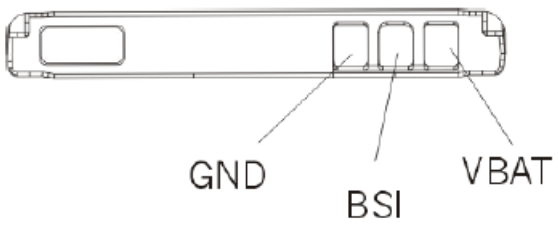


Figure 14: BL-5C battery pack pin order

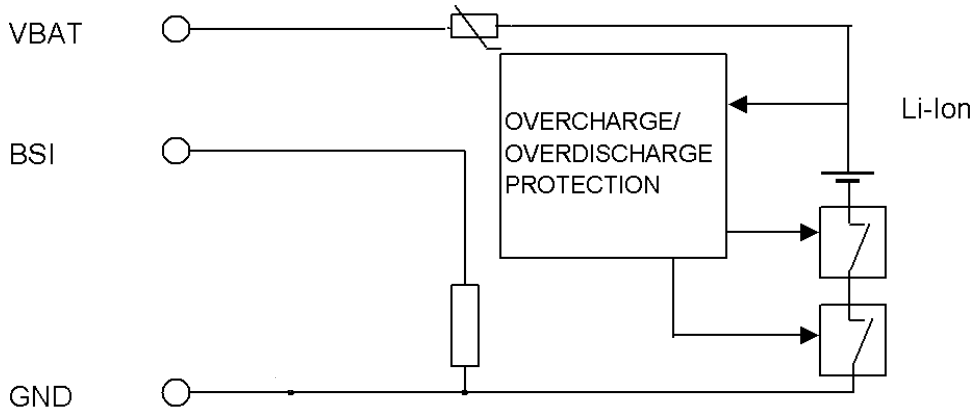


Figure 15: Interconnection diagram inside the battery pack

Charging Circuitry

The UEM ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The RH-48 baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. For the 3-wire charger, the control line is not supported and not connected to the Baseband ASICs. See Figure 16 for details.

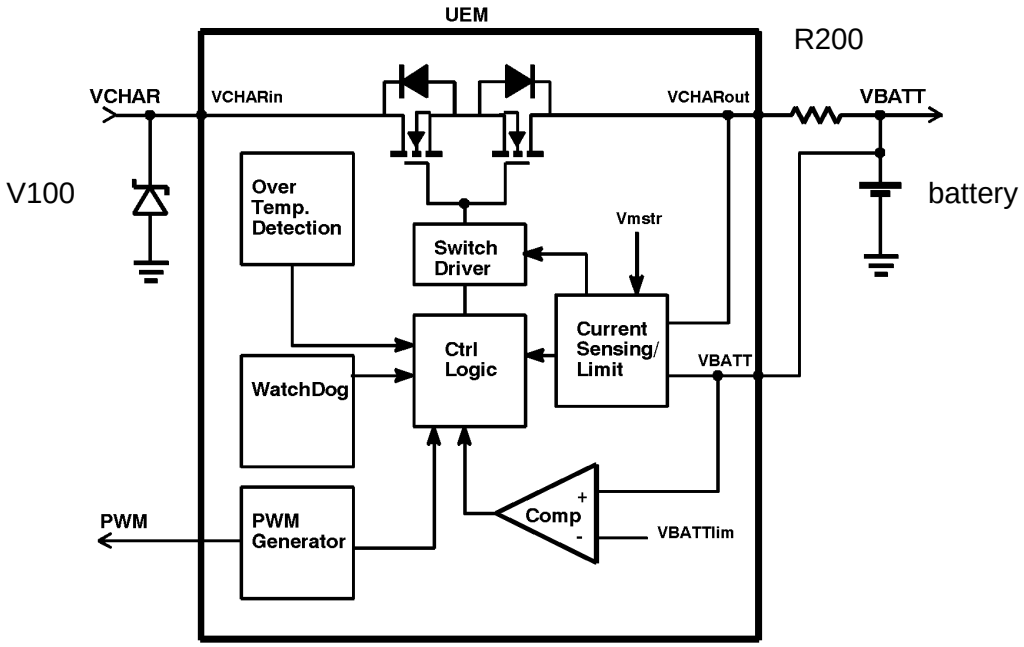


Figure 16: Charging circuitry

Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above 2 V (VCHdet+ threshold) by UEM charging starts. VCHARDET signal is generated to indicate the presence of the charger for the SW. The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

2 Identify the charger as a two-wire or three-wire charger.

3 Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

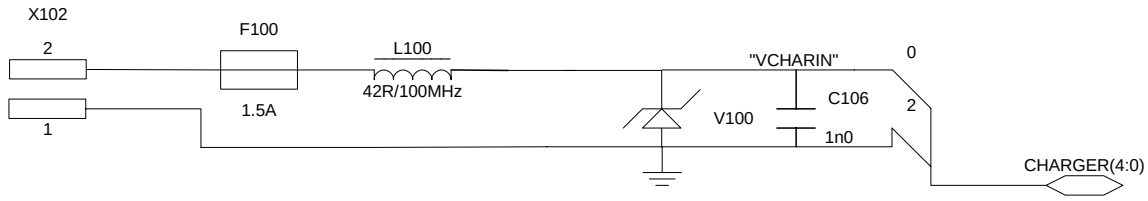


Figure 17: Charging circuit

Charge Control

In active mode, charging is controlled by UEM's digital part. Charging voltage and current monitoring is used to limit charging into safe area. For that reason UEM has programmable charging cut-off limits:

VBATLim1=3.6 V (Default)

VBATLim2L=5.0 V and

VBATLim2H=5.25 V.

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning charging switch OFF. No change in operational mode is done. After voltage has decreased below VBATLim- charging re-starts.

There are two PWM frequencies in use depending on the type of the charger: two-wire charger uses a 1Hz and a three-wire charger uses a 32Hz. Duty cycle range is 0% to 100%. Maximum charging current is limited to 1.2 A.

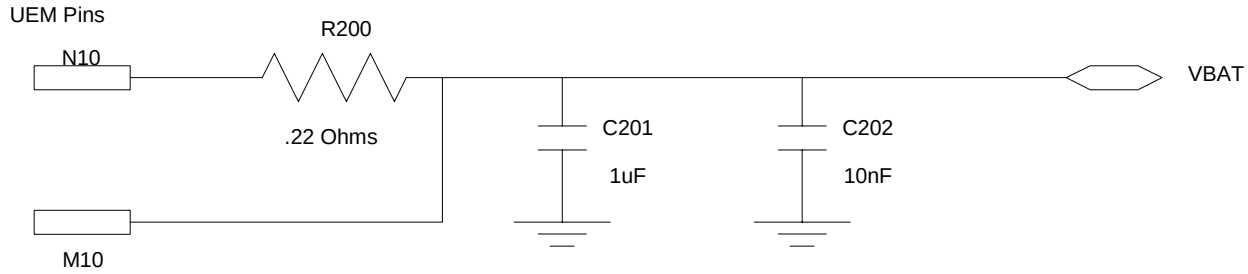


Figure 18: Charging circuity at the battery

Audio

The audio control and processing in RH-48 is provided by UEM, which contains the audio codec, and UPP — which contains the MCU and DSP blocks, handling and processing the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the phone's internal microphone; MIC2 input is used for headsets (HDB-4). MIC3 is not used. Every microphone input can have either a differential or single-ended AC connection to UEM circuit. In RH-48, the internal microphone (MIC1) and external microphone (MIC2) for Tomahawk accessory detection are both differential. The microphone signals from different sources are connected to separate inputs at UEM. Inputs for the microphone signals are differential type. Also, MICBIAS1 is used for MIC1 and MICBIAS2 is used for MIC2.

Display and Keyboard

LEDs are used for LCD and keypad illumination in RH-48. There are two LEDs for LCD and four LEDs for keypad. The signal used to drive the LED driver for the LCD and keyboard is KLIGHT. This signal turns on the LED driver (N302).

Color LCD is used in RH-48. Interface is using 9-bit data transfer. The interface is quite similar to DCT3 type interface, except Command/Data information is transferred together with the data.

The following figure is the waveform for LCD interface.

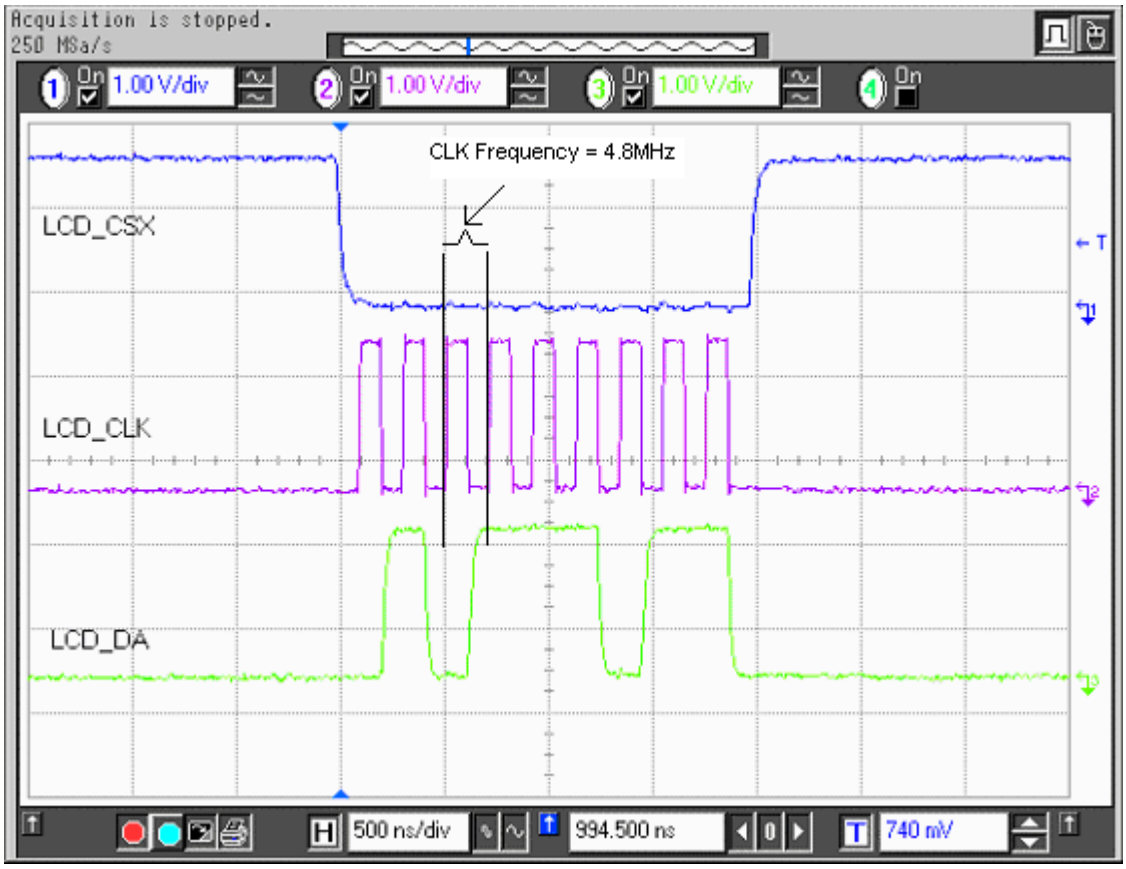


Figure 19: LCD Interface

Accessory

RH-48 supports Tomahawk and Universal Headset accessories, differential and single-ended, respectively. Detection of Tomahawk accessories is done through the ACI signal where the Universal Headset is detected on GenIO (12). The following graphic shows the pin out of the Tomahawk connector.

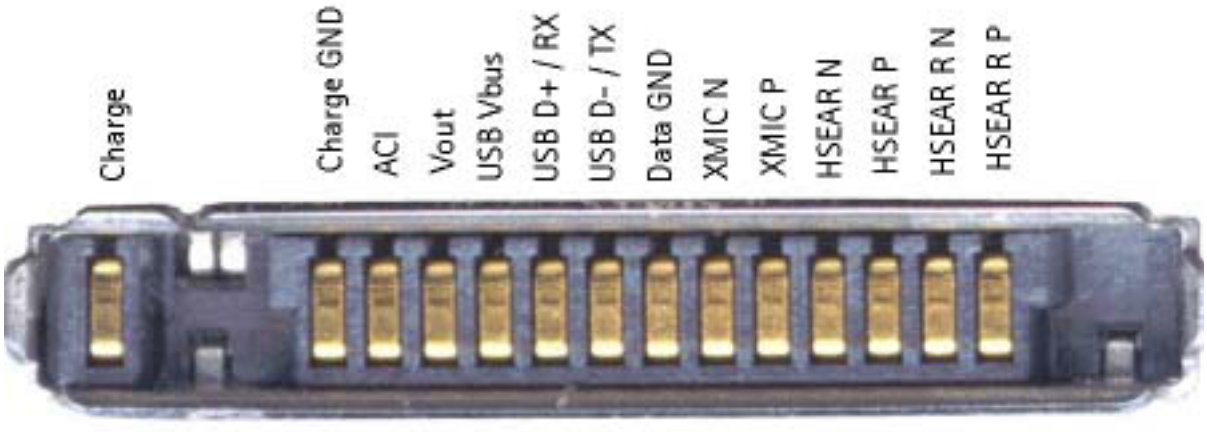


Figure 20: Tomahawk pin out

The pin out on the Tomahawk connector is as follows:

1. Charger
2. Charger GND
3. ACI
4. Vout
5. USB Vbus
6. USB D+ / Fbus Rx
7. USB D- / Fbus Tx
8. Data GND
9. XMic N
10. XMic P
11. HSear N
12. HSear P
13. HSear R N
14. HSear R P

In Tomahawk accessories, the following functions may be performed: charging, accessory detection, FBUS communication, USB communication, and fully differential audio interface for mono- and stereo outputs.

Charging

Charging through the Tomahawk is accomplished in the same manner as through the charger connector. Pin 1 of the Tomahawk is physically connected to the charger connector. When the phone is connected to a desktop charger (*e.g.*, DCV-15), it charges in the same manner as it does with the charger connector.

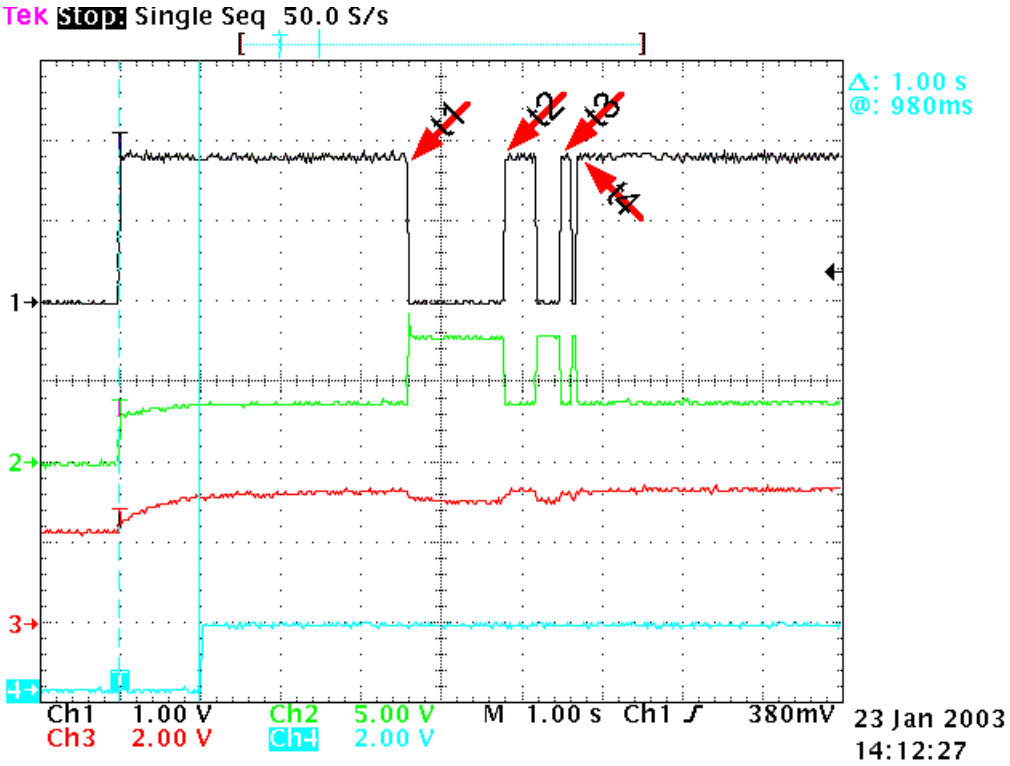
The actual charging sequence is illustrated in the following diagram. The channels on the diagram are:

CH1 = Charging current across the .22 Ohm (R200) resistor on UEMK

CH2 = Charger voltage measure at V100

CH3 = Battery voltage measure at R200

CH4 = PURX



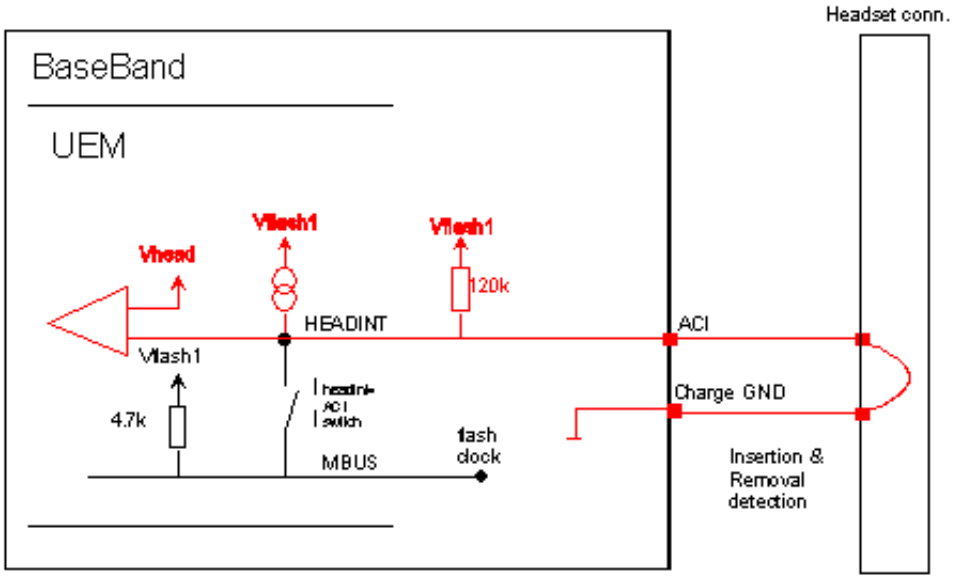
t1: UEM opens charge switch and UPP startup.
t2: This is very very early in phone SW startup where the charge switch is being closed. Charge switch remains closed during OS and server startup to prevent HW cut-off.
t3: EM SW is started and charger recognition SW verifies charger current.
t4: Charger is accepted and Constant Current charging is started.

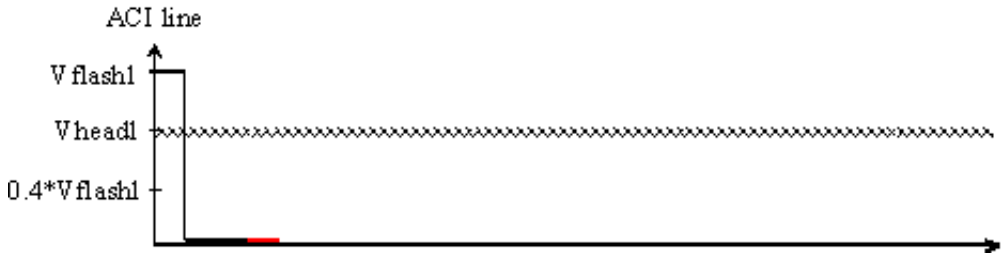
In Channel 4 PURX is released; this indicates when the phone operation goes from "RESET" mode to "POWER_ON" mode.

Tomahawk Headset Detection

Accessory detection on the Tomahawk is done digitally. The pins used for this accessory detection are:
Pin 2 (Charge GND)
Pin 3 (ACI)
Pin 4 (Vout)

A waveform depicting such detection follows:

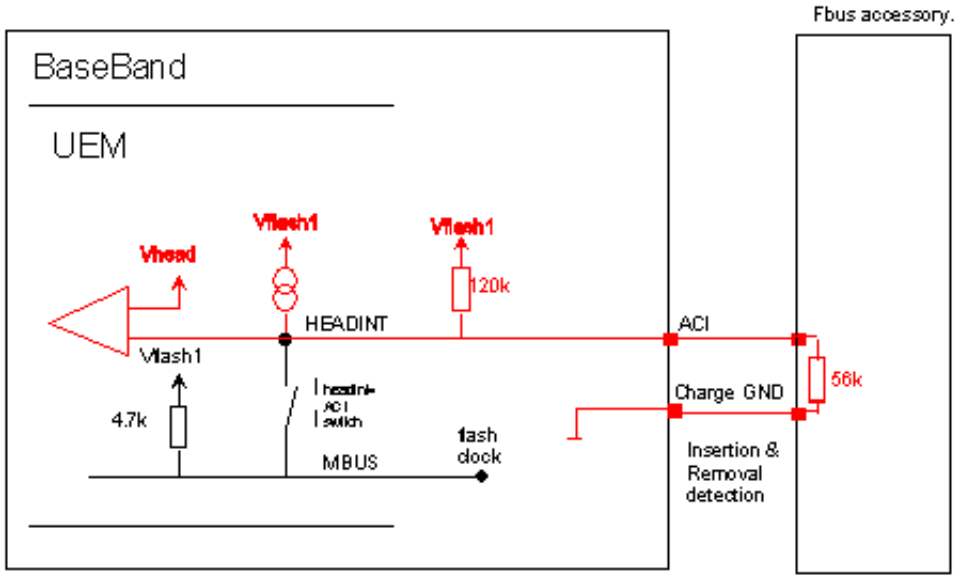


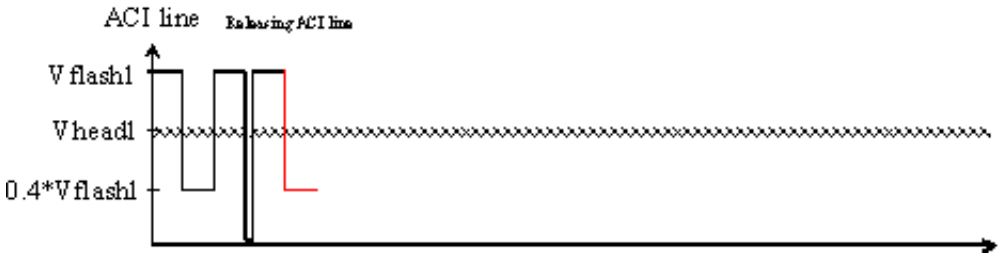


FBus Detection

FBus communication in Tomahawk is done through the following lines:
Pin 2 (Charge GND)
Pin 3 (ACI)
Pin 4 (Vout)
Pin 6 (FBus Rx)
Pin 7 (FBus Tx)

A waveform for such communication is illustrated here:



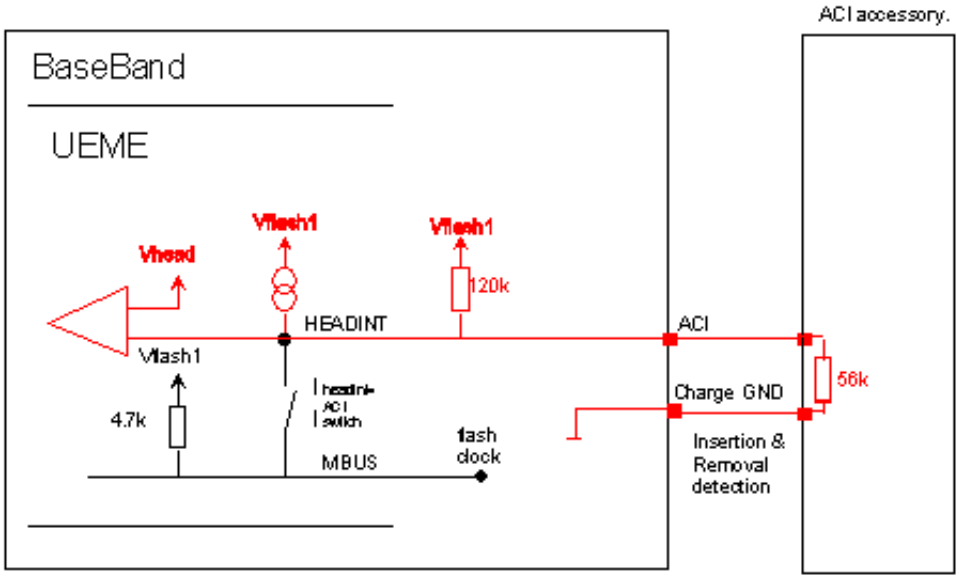


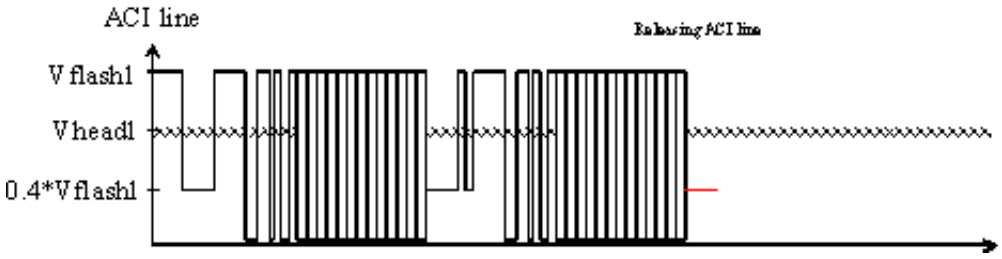
Accessory Detection Through ACI

USB and Audio on (mono or stereo) and FM radio communication in Tomahawk is done through the following signals:

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

A waveform showing this interface follows:





SIM CAR

RH-48 supports SIM CAR. The following waveform may be used to verify that sim_vcc; sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture may be taken when the SIM CAR is installed on the phone to measure the signals when the phone is turned on. The diagram shows the proper waveforms when the interface is working. See Figure 23 (bottom view) diagram for the test point's location.

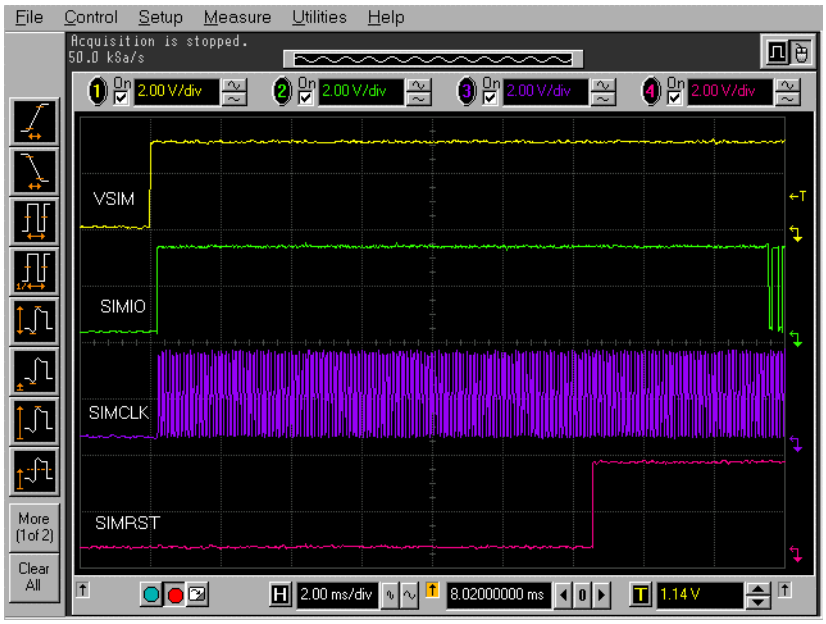


Figure 21: RUIM Signal Waveform

Test Points

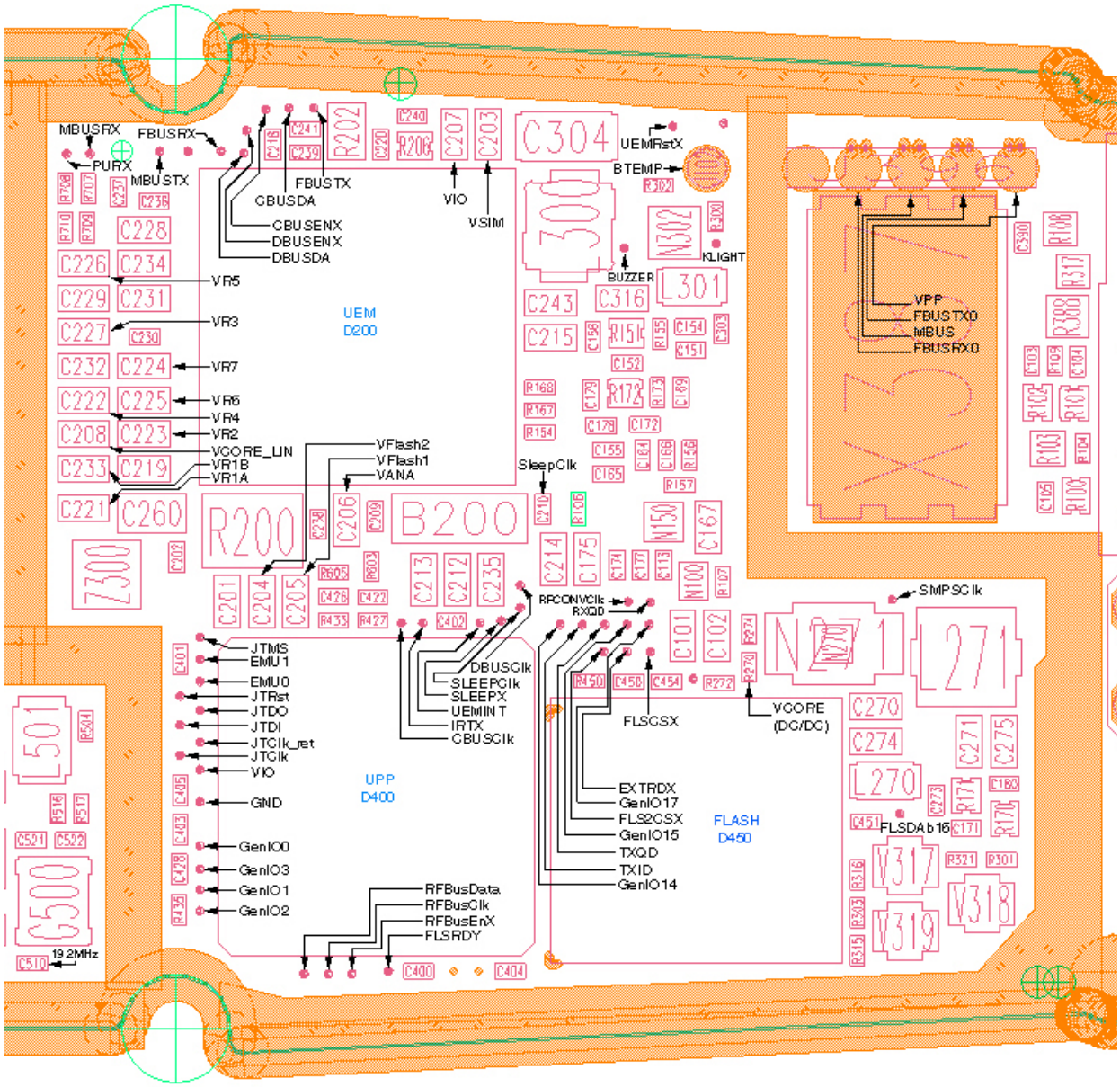


Figure 22: RH-48 BB test points, regulators, and BB ASICs

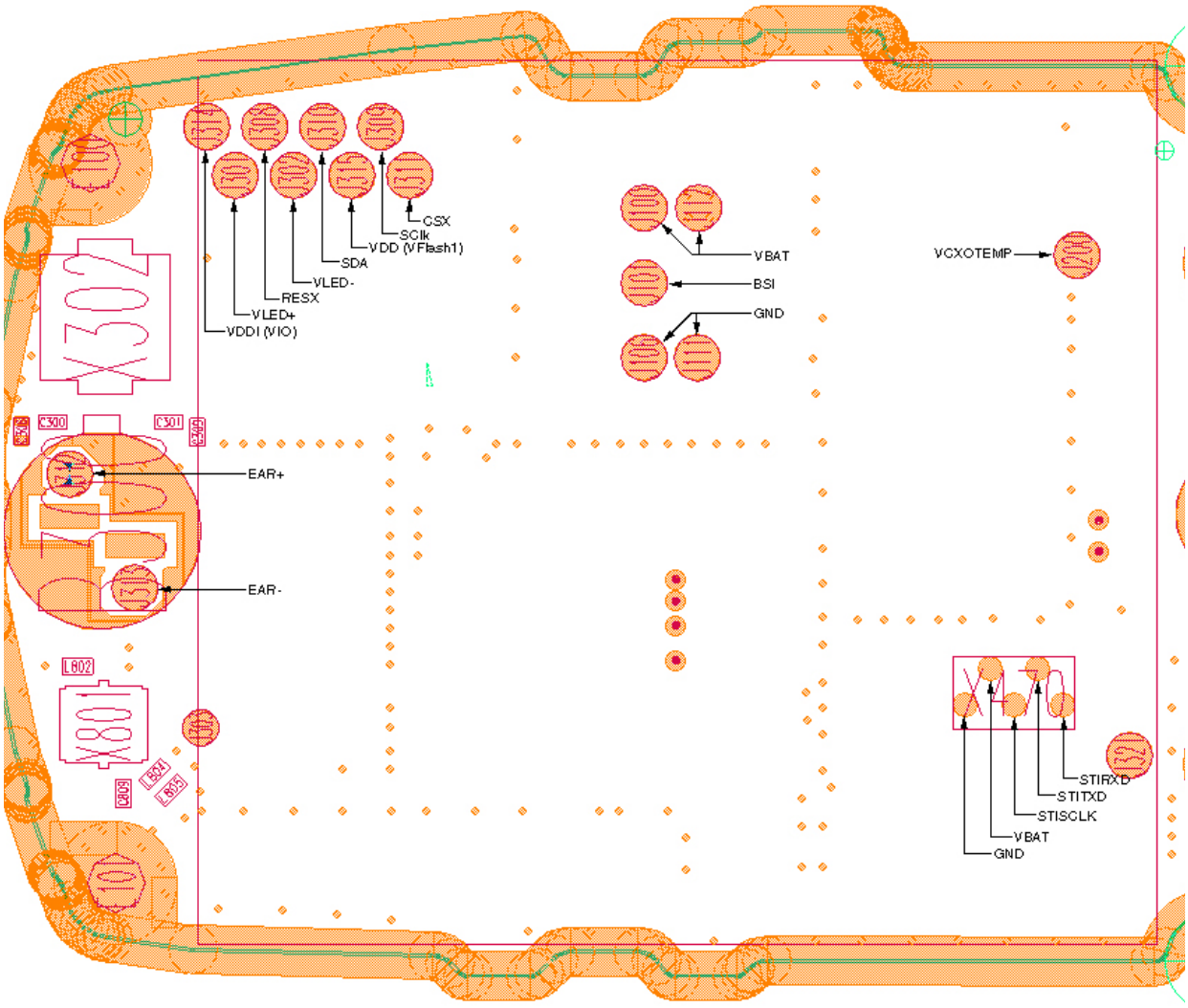


Figure 23: RH-48 BB test points, regulators, and BB ASICs

Troubleshooting

The following hints should help finding the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided following sections:

1 Top troubleshooting map

2 Phone is totally dead

3 Power doesn't stay on or the phone is jammed

4 Flash programming doesn't work

5 Display is not working

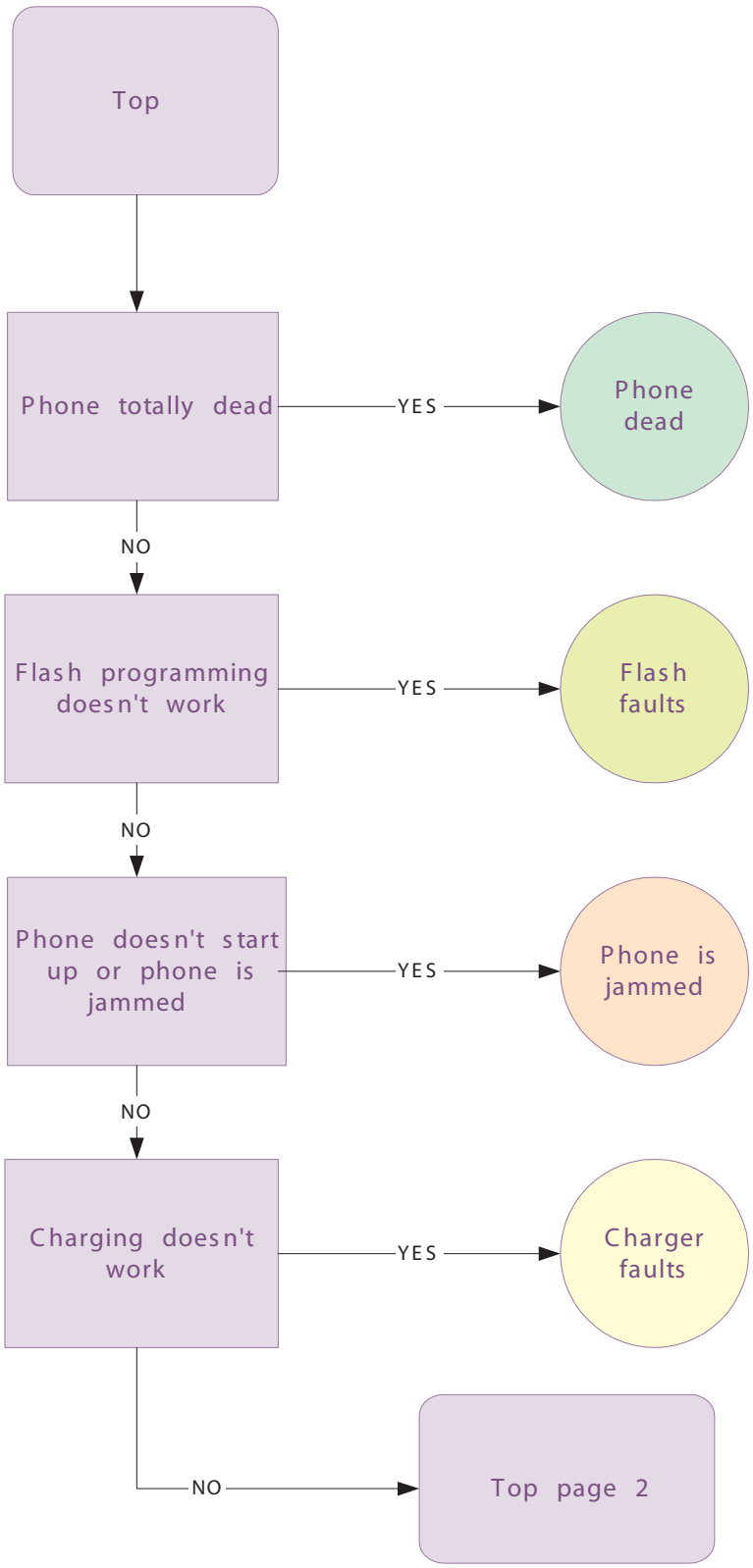
6 Audio fault

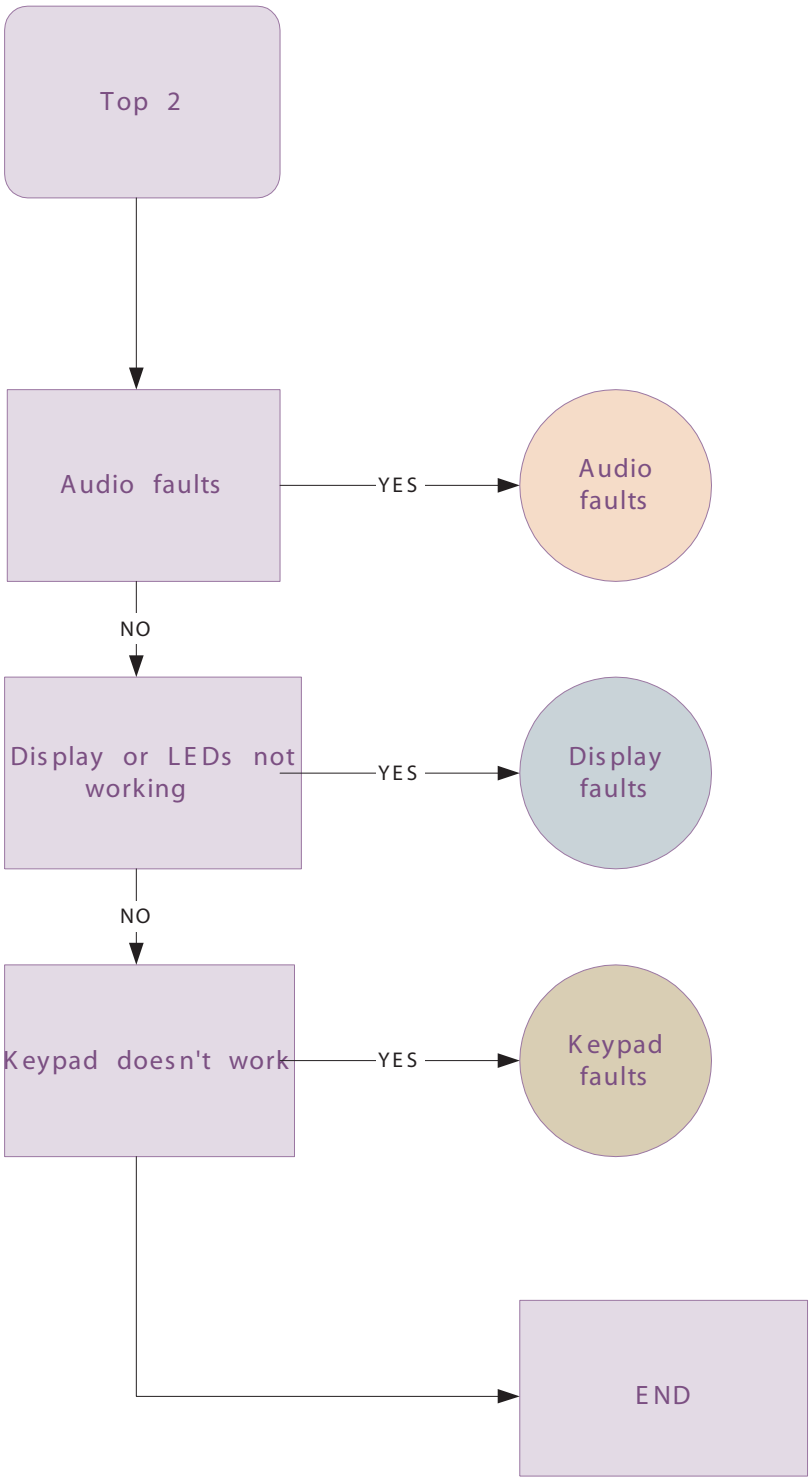
7 Charging fault

First, carry out a through visual check of the module. Ensure in particular that:

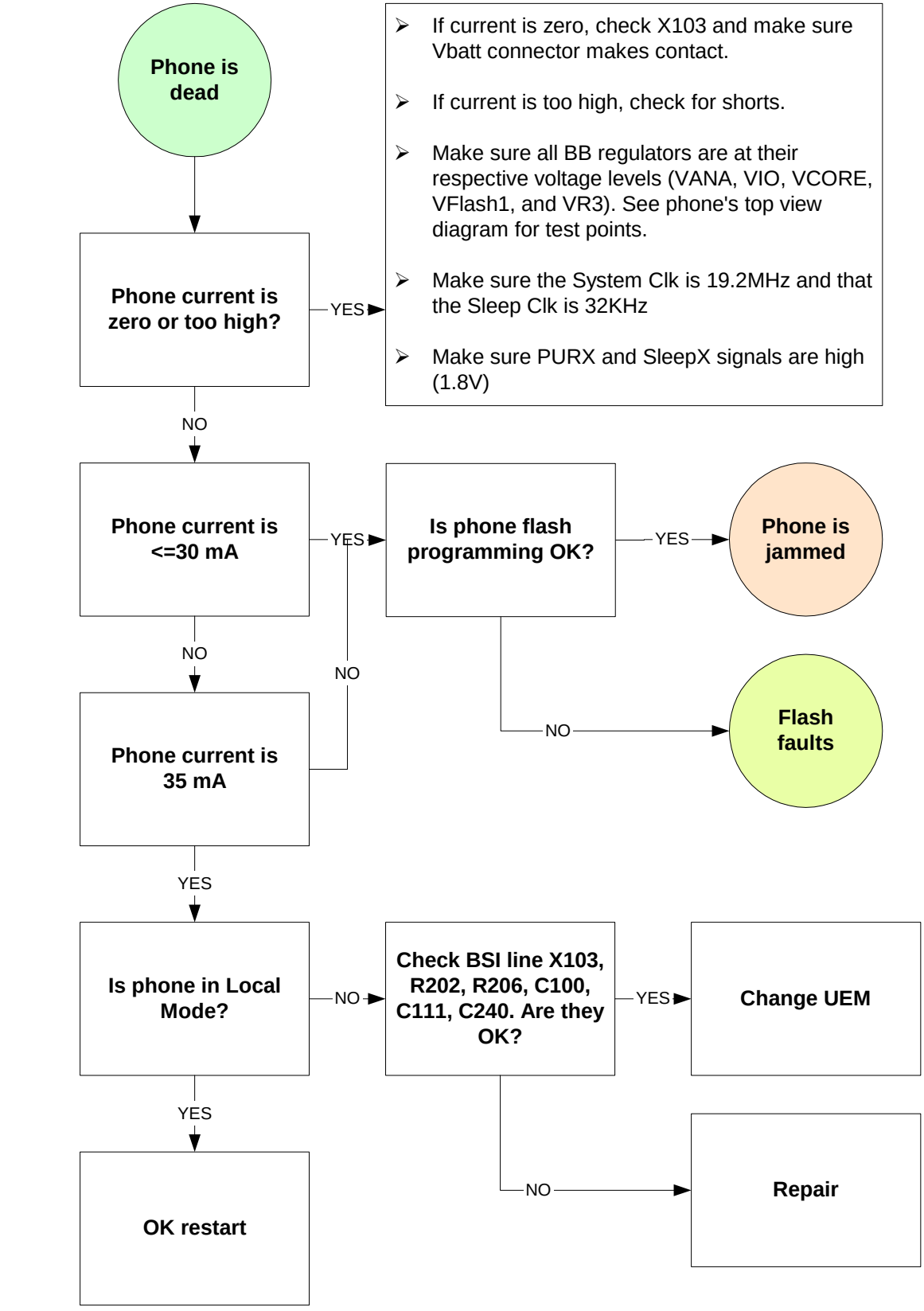
- there are no mechanical damages
- soldered joints are OK
- ASIC orientations are OK

Top troubleshooting map

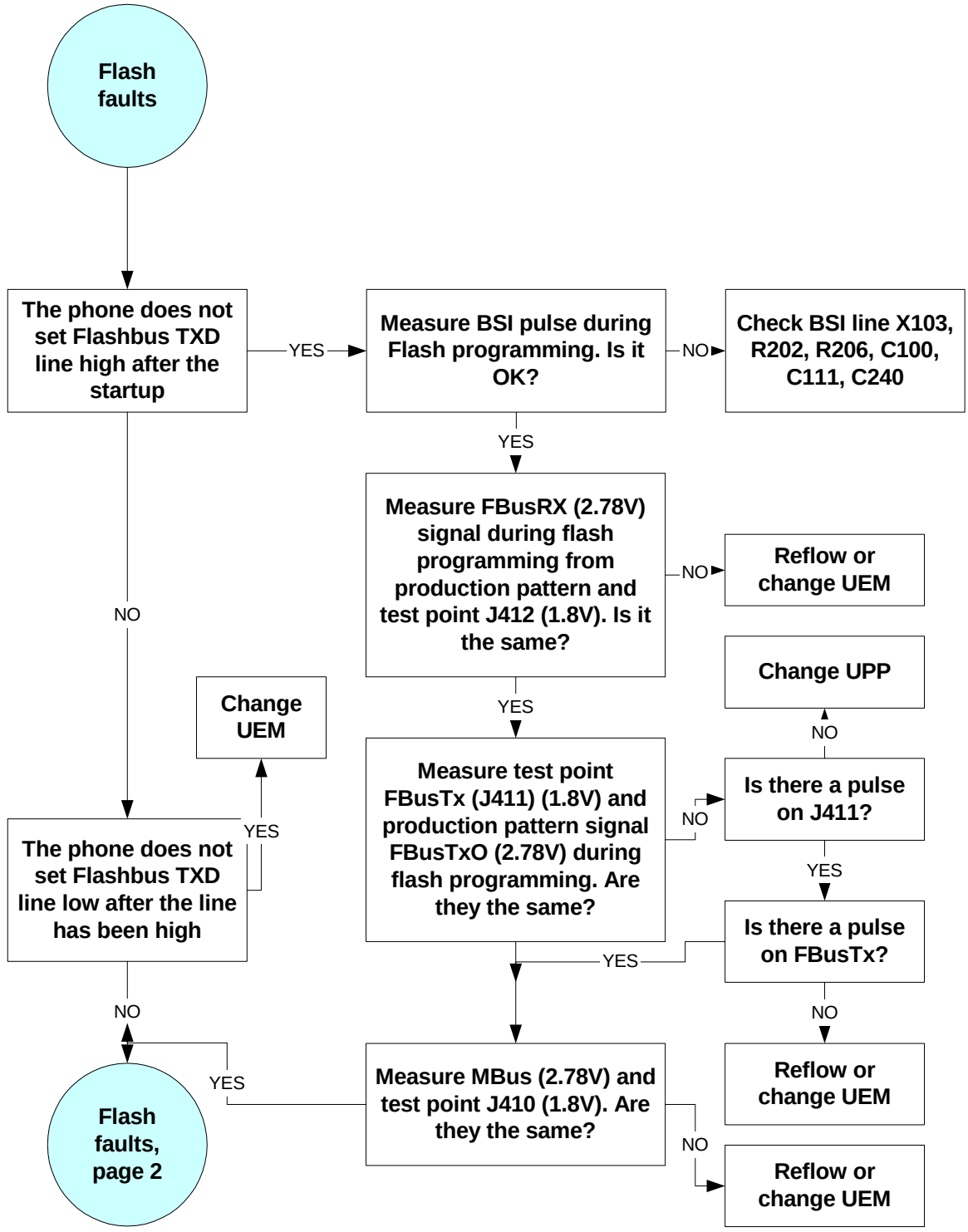


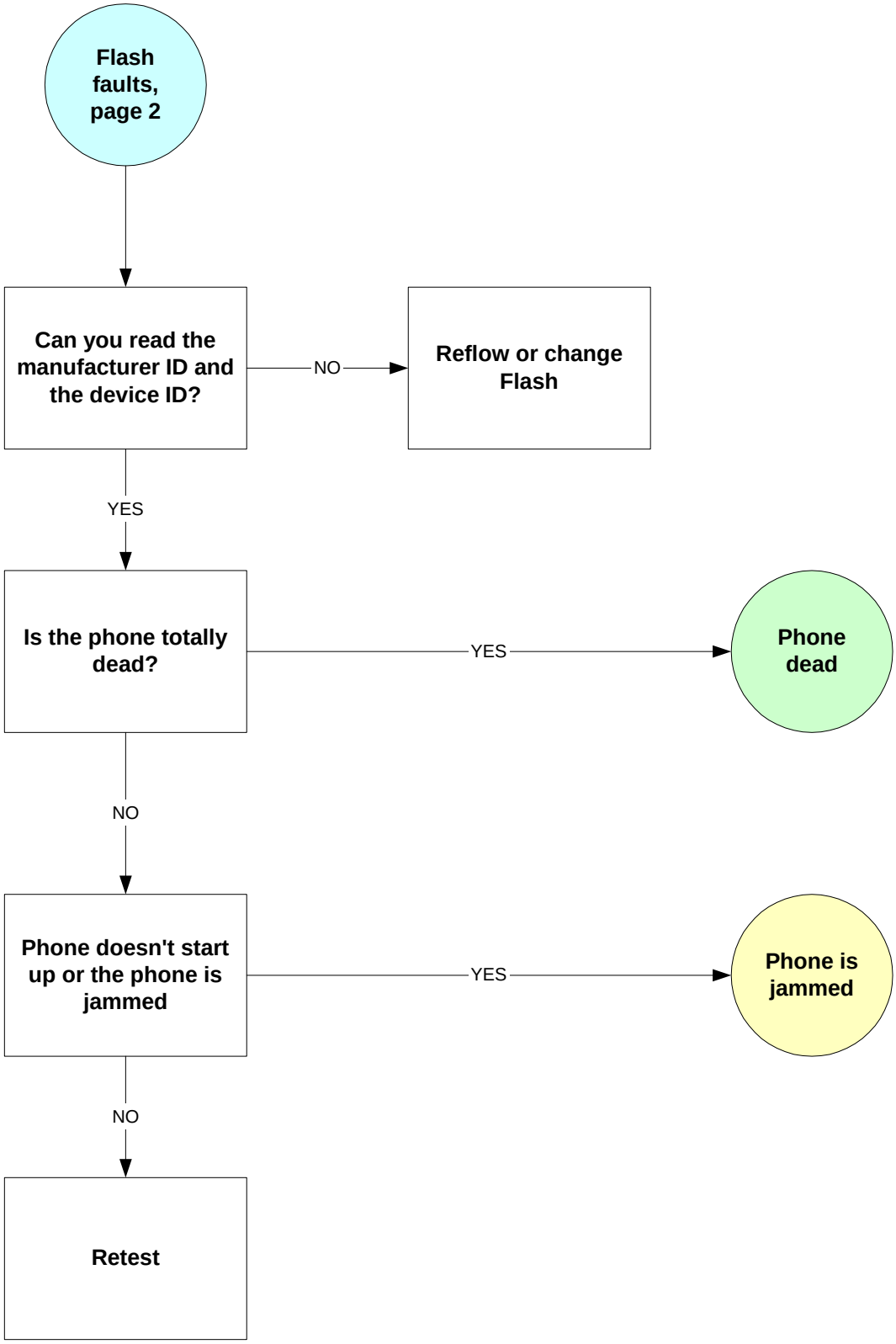


Phone is totally dead

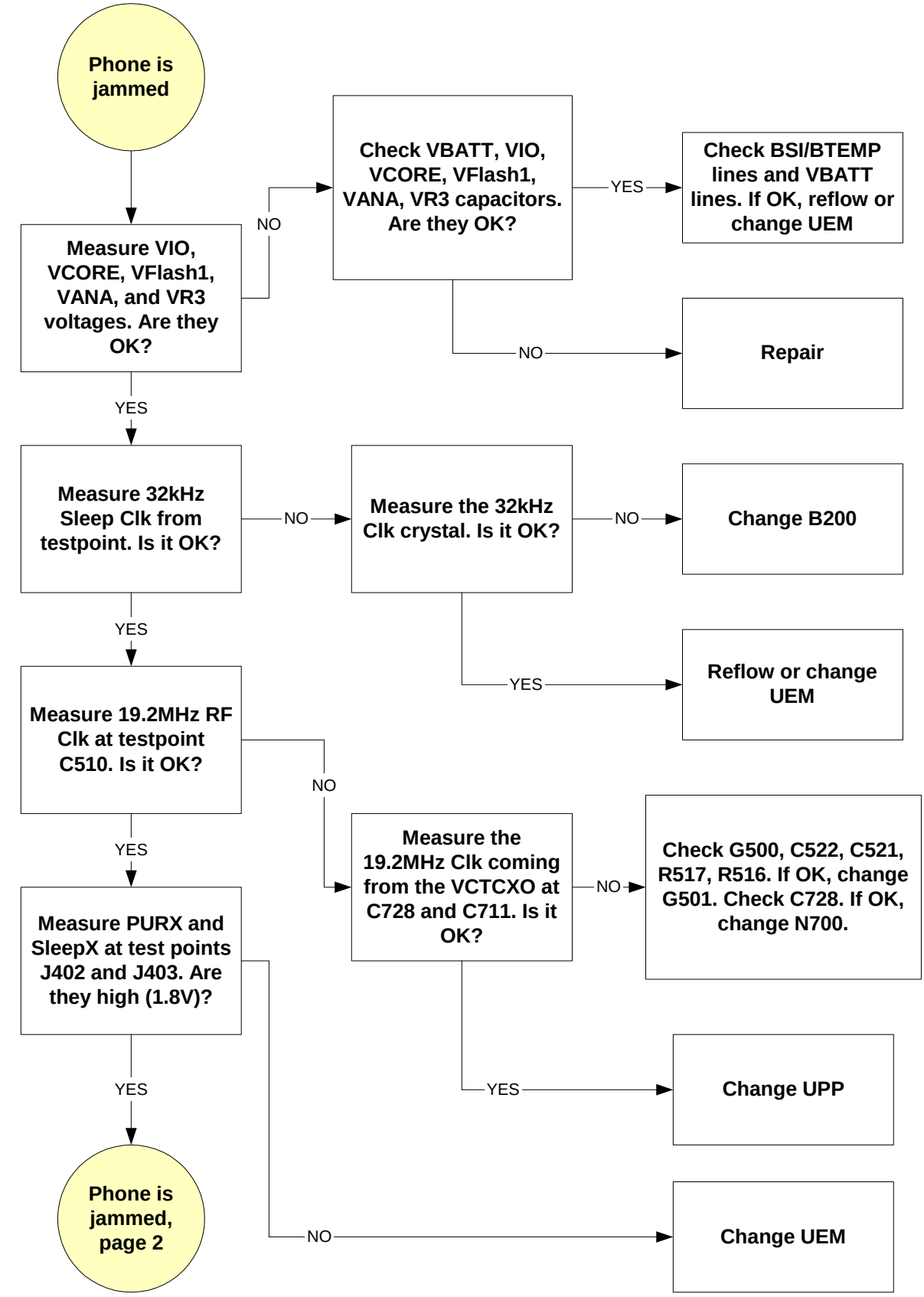


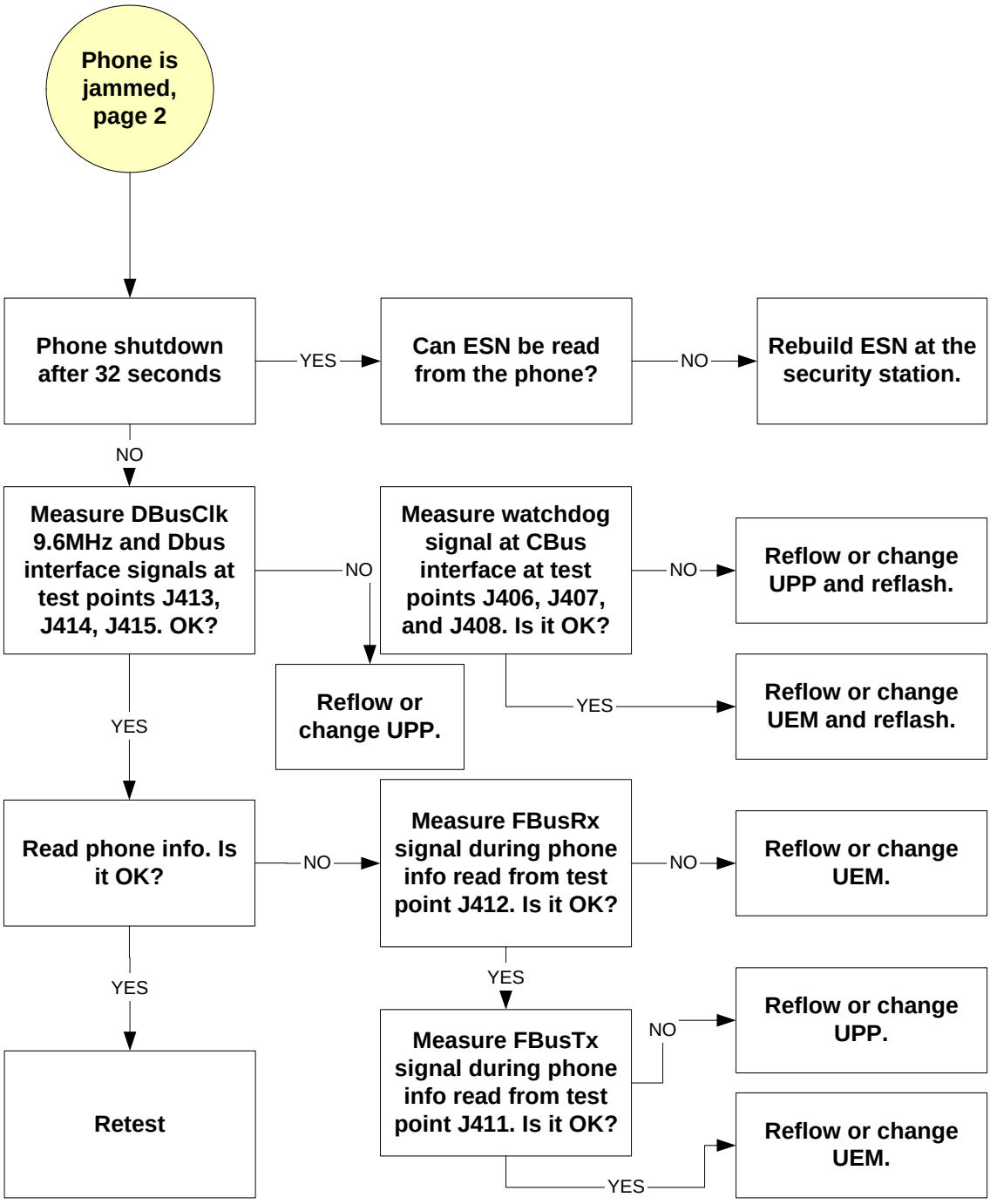
Flash programming doesn't work



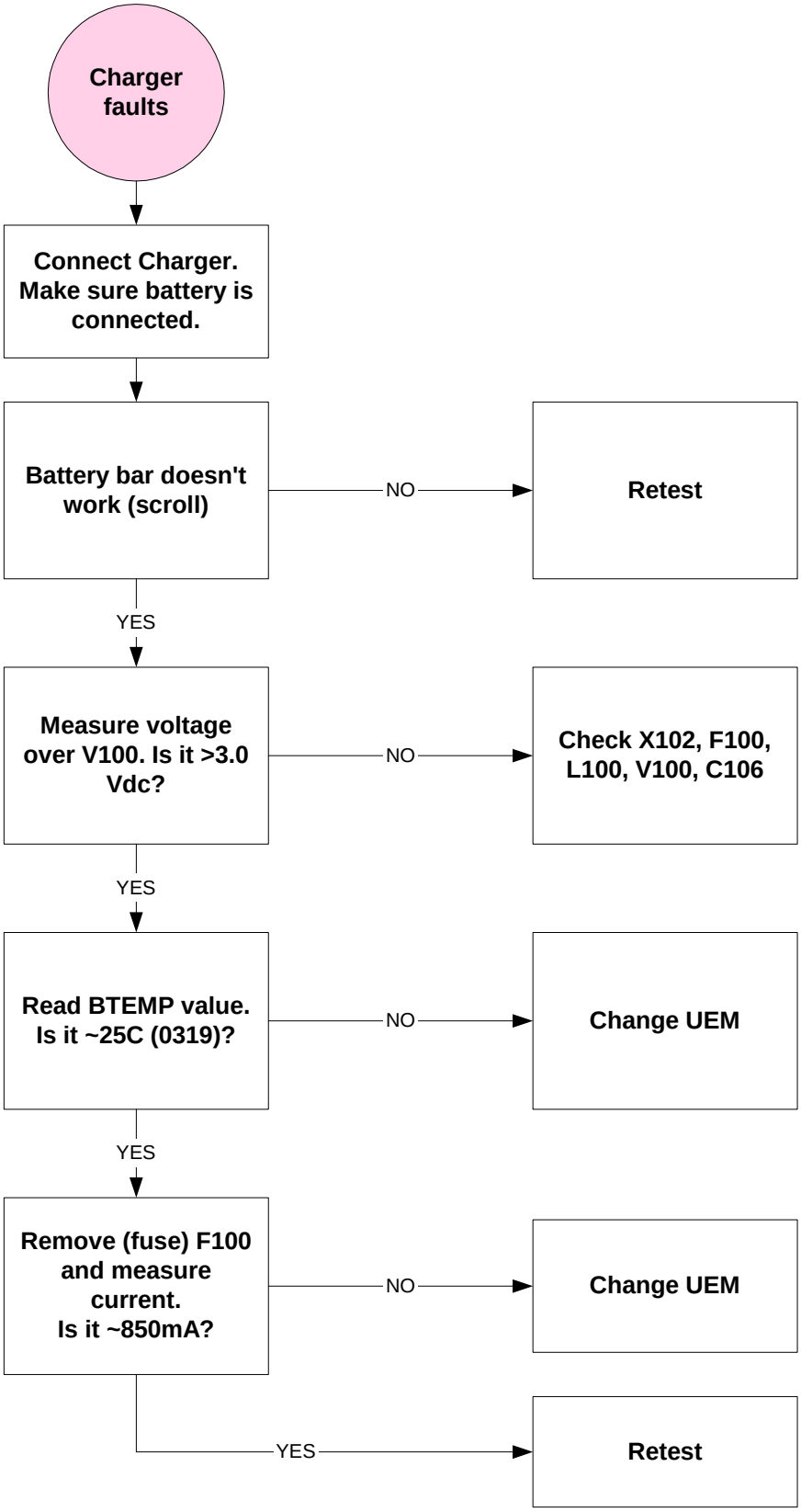


Power doesn't stay on or the phone is jammed

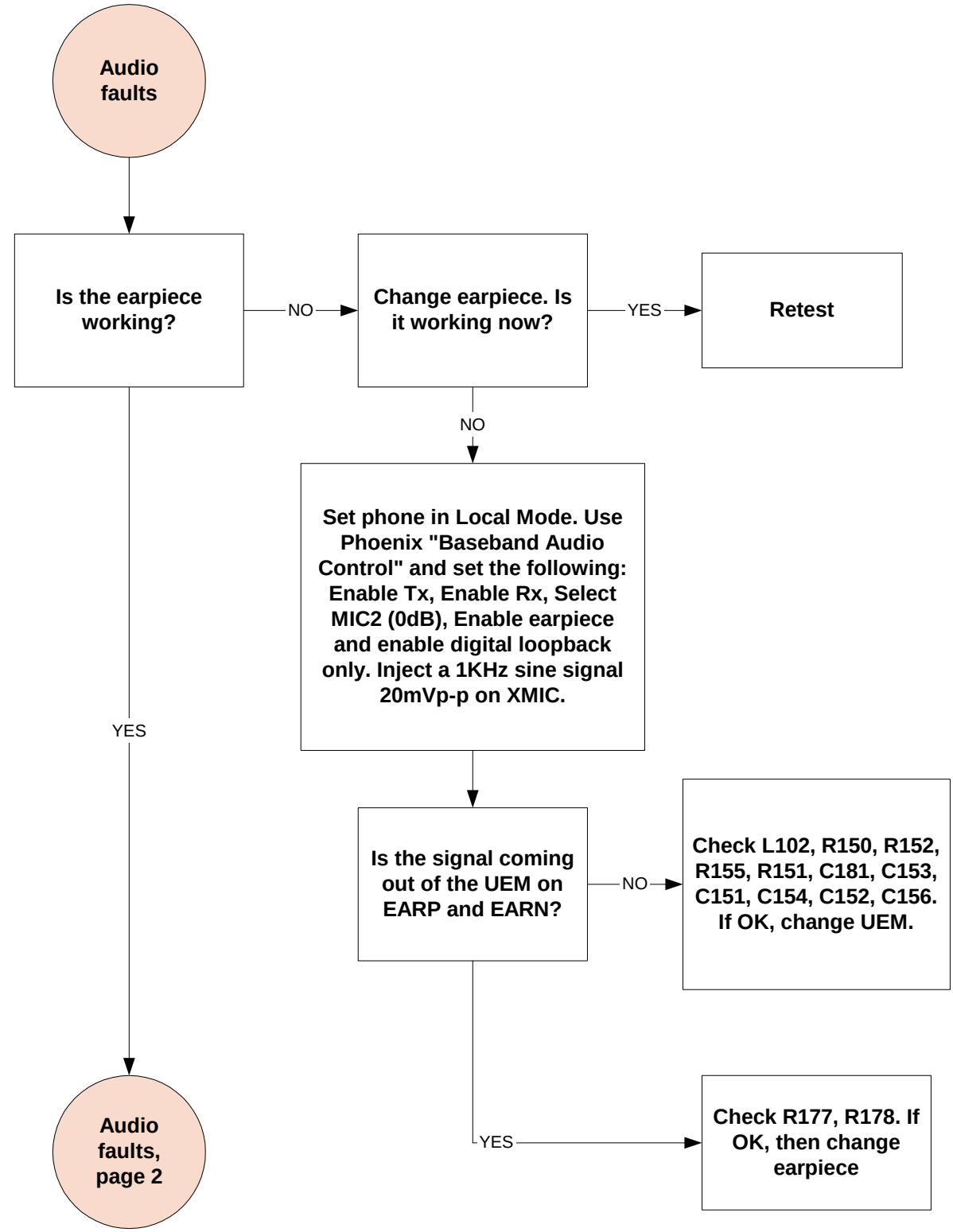


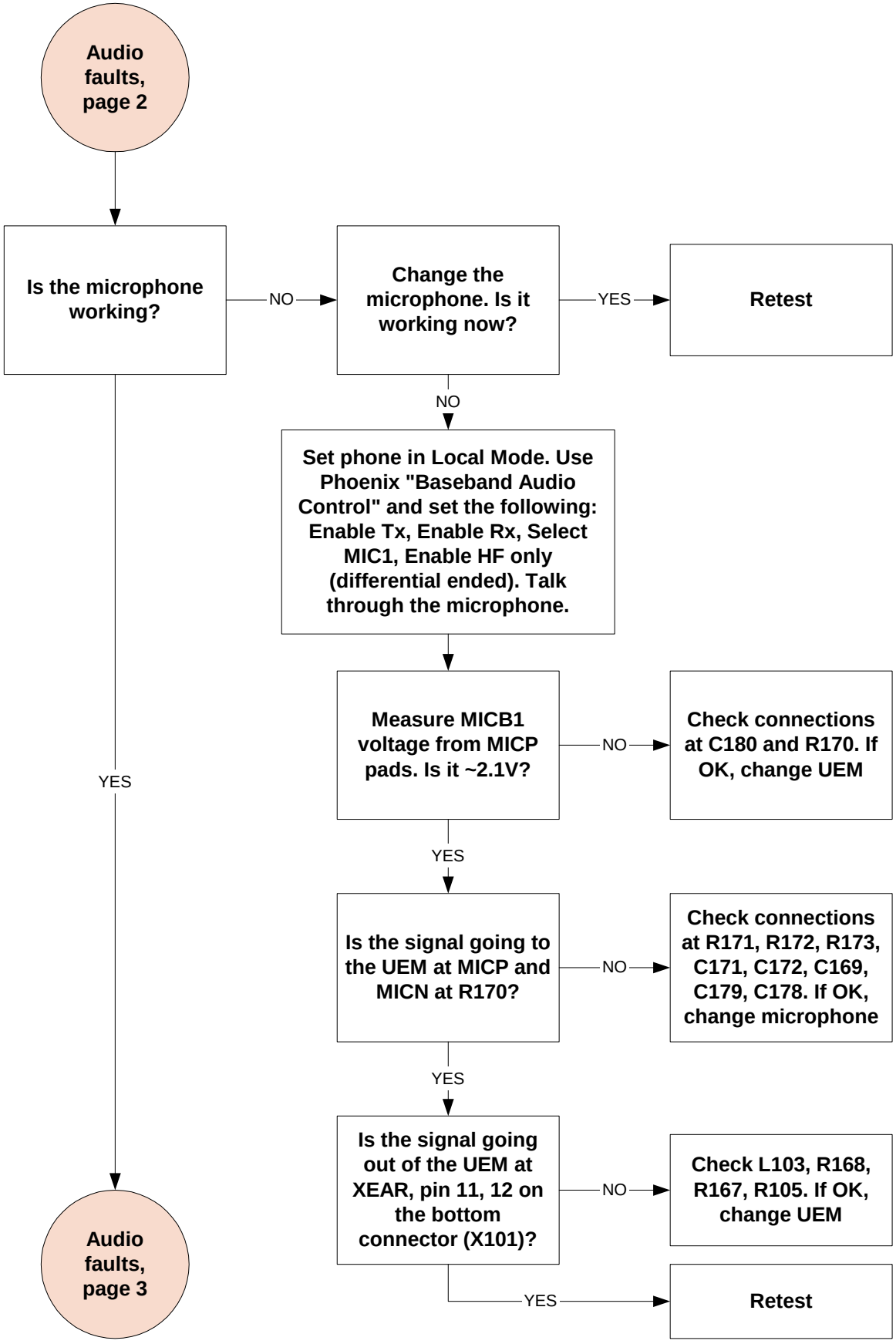

Phone is jammed, page 2
Phone shutdown after 32 seconds
YES
Can ESN be read from the phone?
NO
Rebuild ESN at the security station.
NO
Measure DBusClk 9.6MHz and Dbus interface signals at test points J413, J414, J415. OK?
NO
Measure watchdog signal at CBus interface at test points J406, J407, and J408. Is it OK?
NO
Reflow or change UPP and reflash.
YES
Reflow or change UEM and reflash.
Reflow or change UPP.
YES
Read phone info. Is it OK?
NO
Measure FBusRx signal during phone info read from test point J412. Is it OK?
NO
Reflow or change UEM.
YES
YES
Measure FBusTx signal during phone info read from test point J411. Is it OK?
NO
Reflow or change UPP.
Retest
YES
Reflow or change UEM.

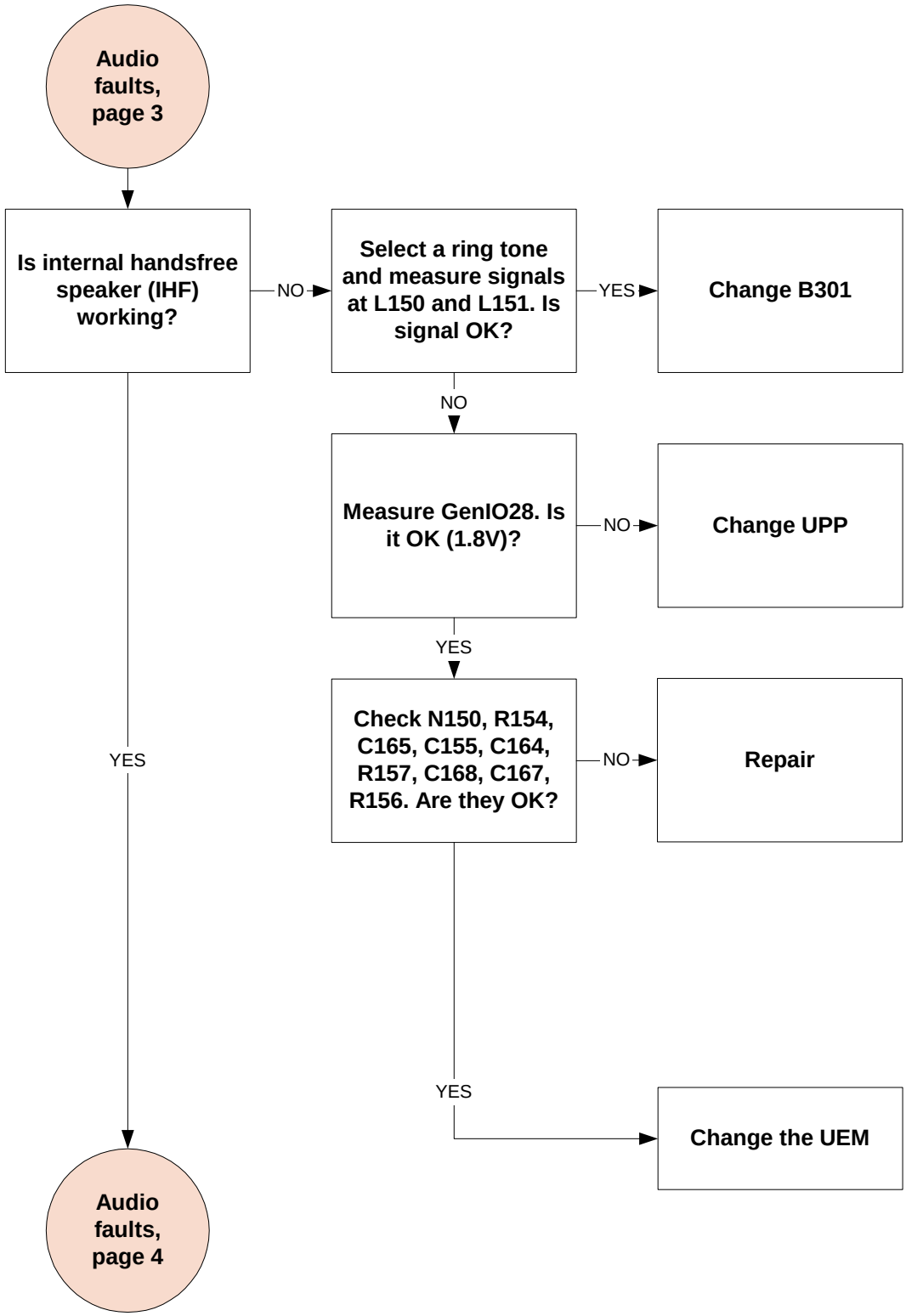
Charger

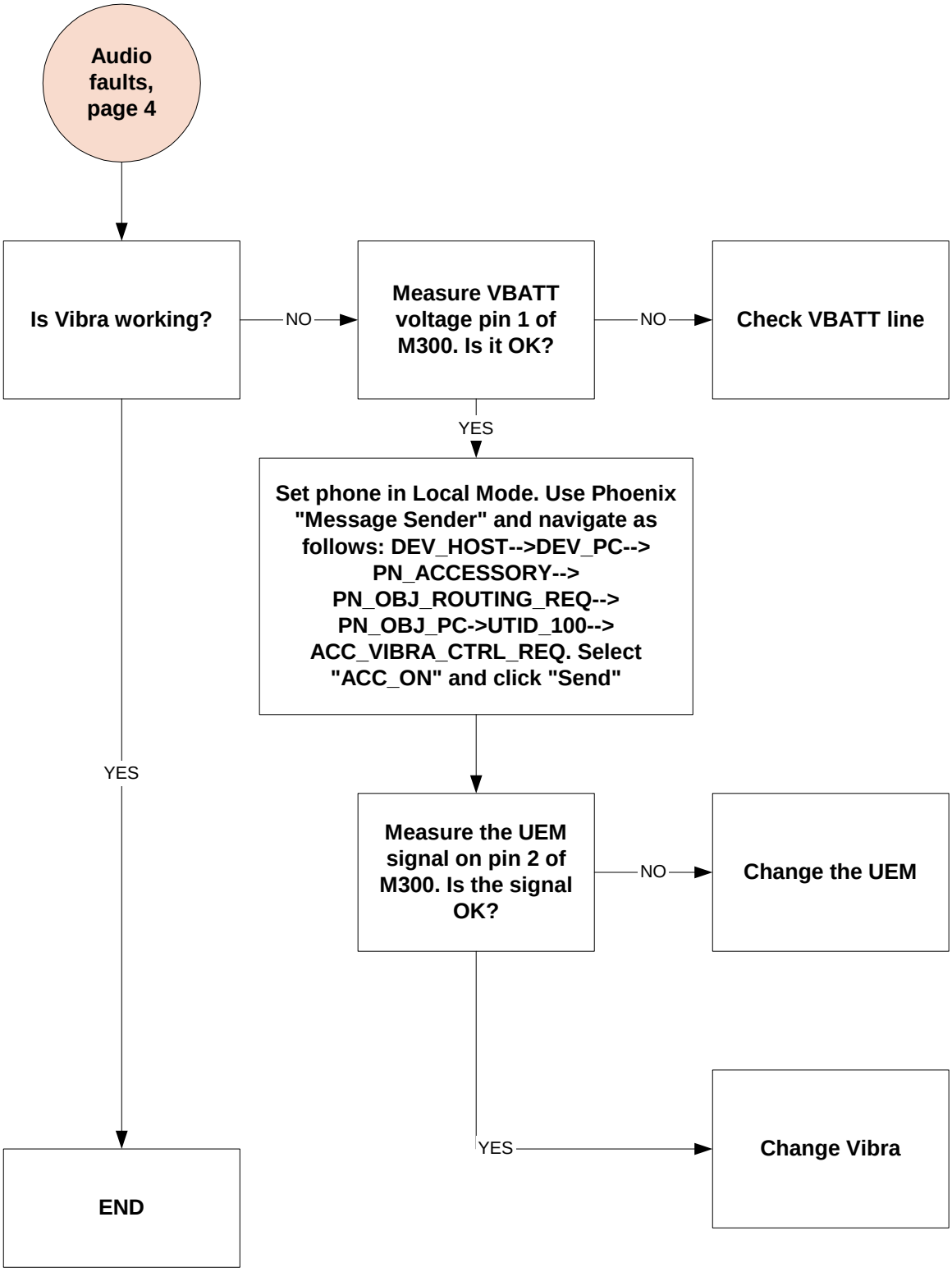


Audio faults

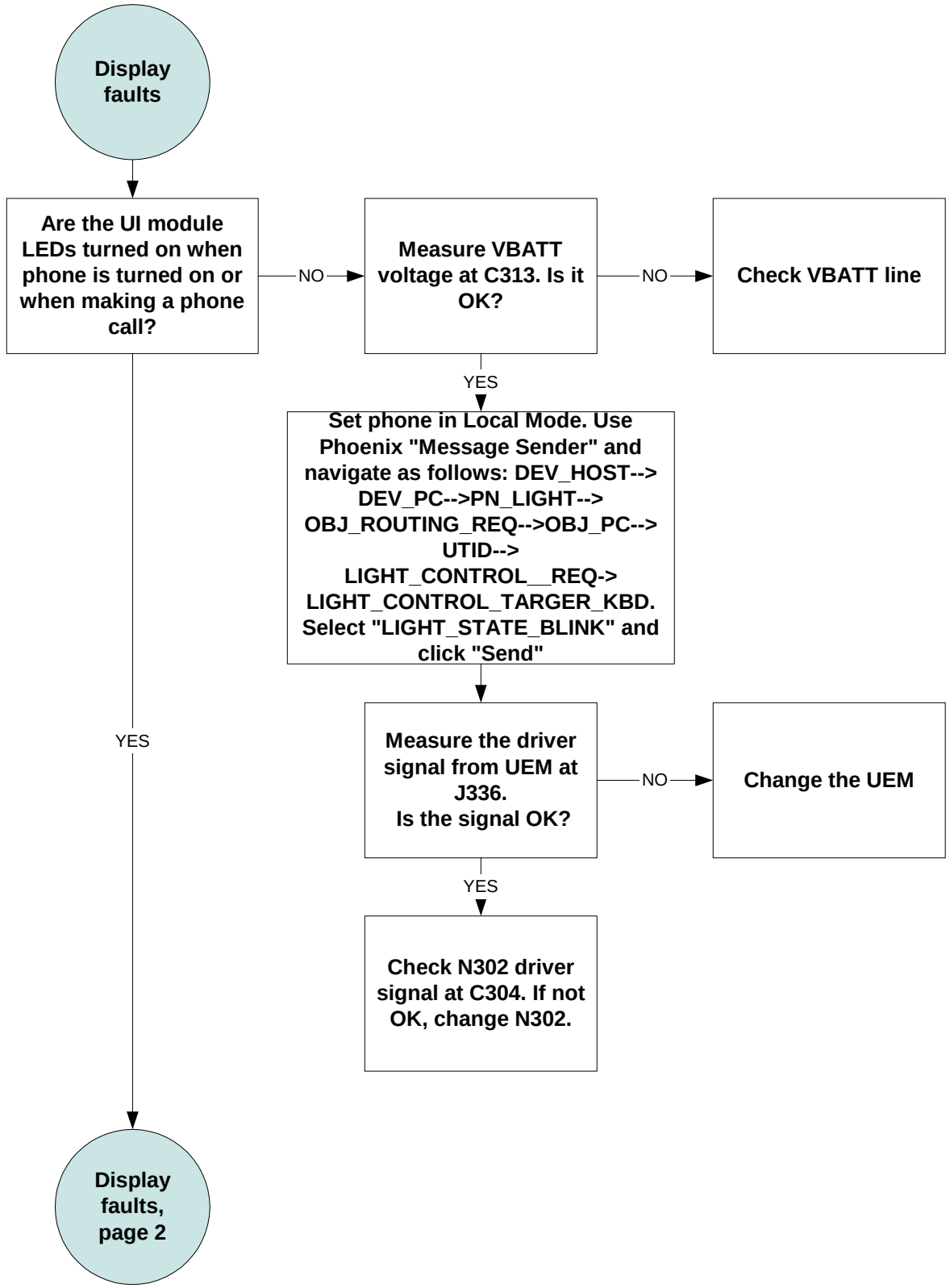


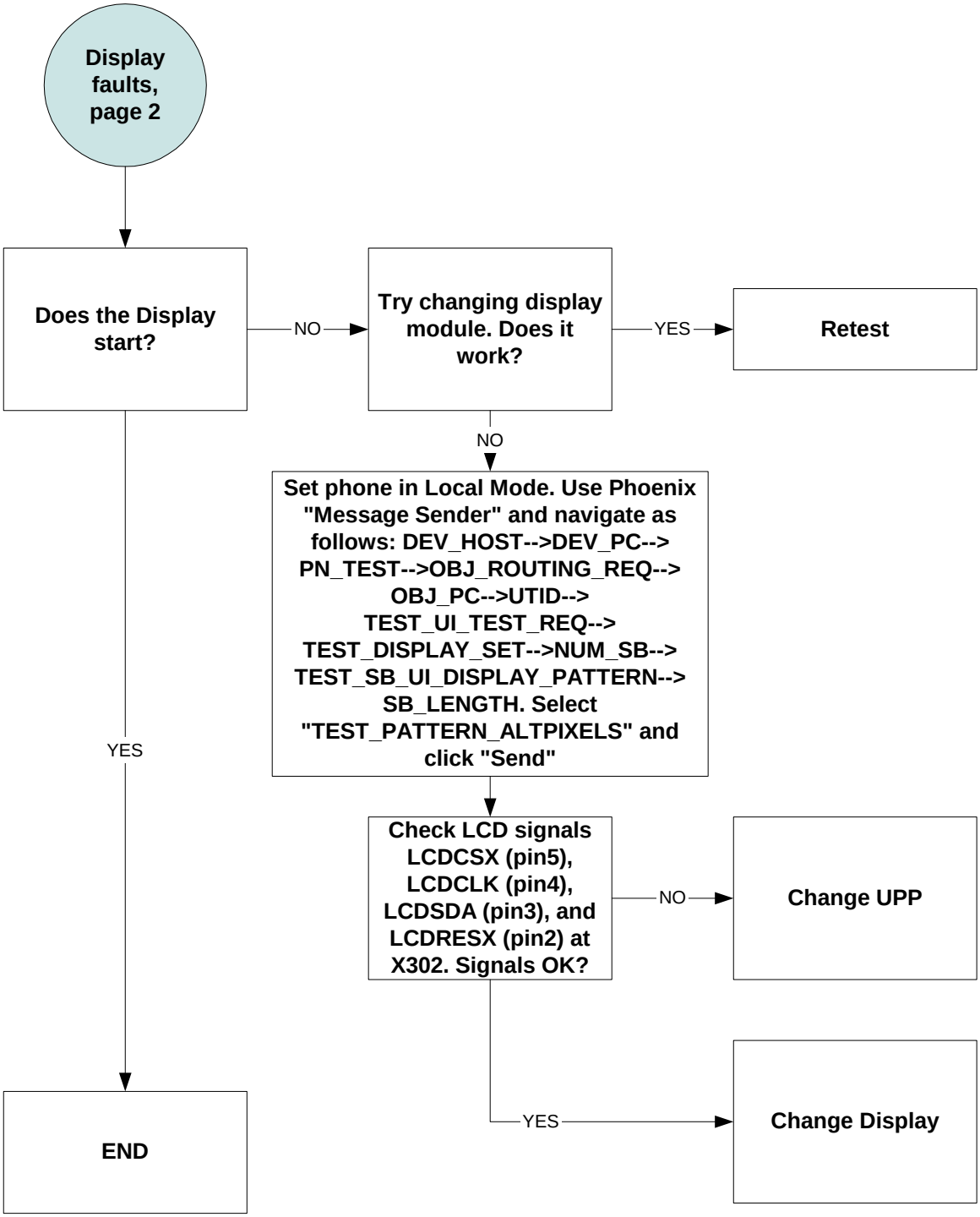






Display faults





Keypad faults